

1981-12-14

CONSTRUCTION OF A PACKET RADIO NODE
CONTROL COMPUTER

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INTERNAL REPORT
LiTH-ISY-I-0491



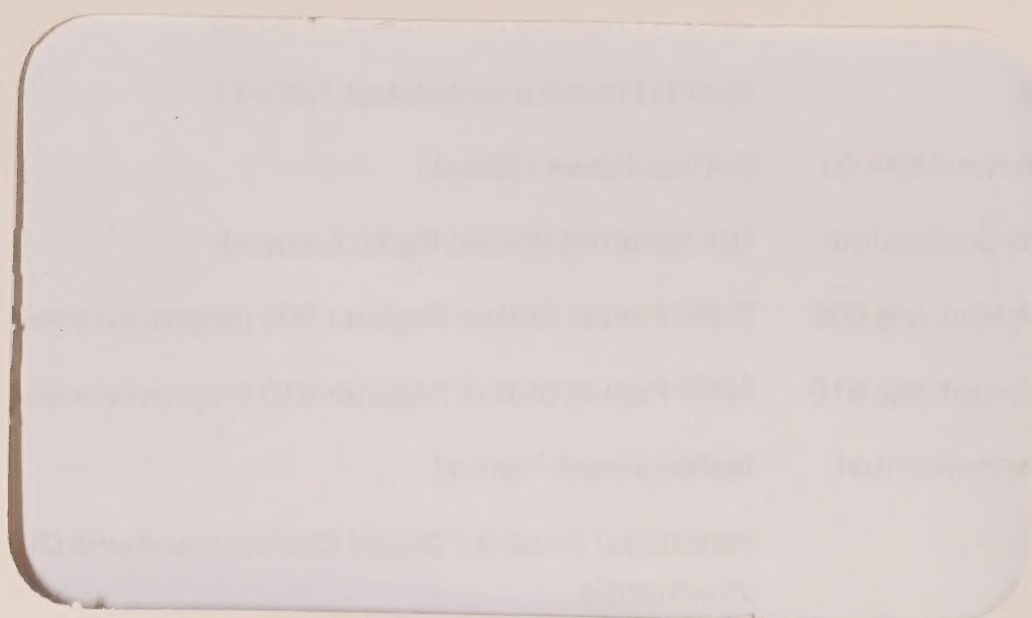


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1. INTRODUCTION

An experimental packet-radio network is under construction at the university of Linköping. It is a distributed network with all nodes programmable via the network under normal operation.

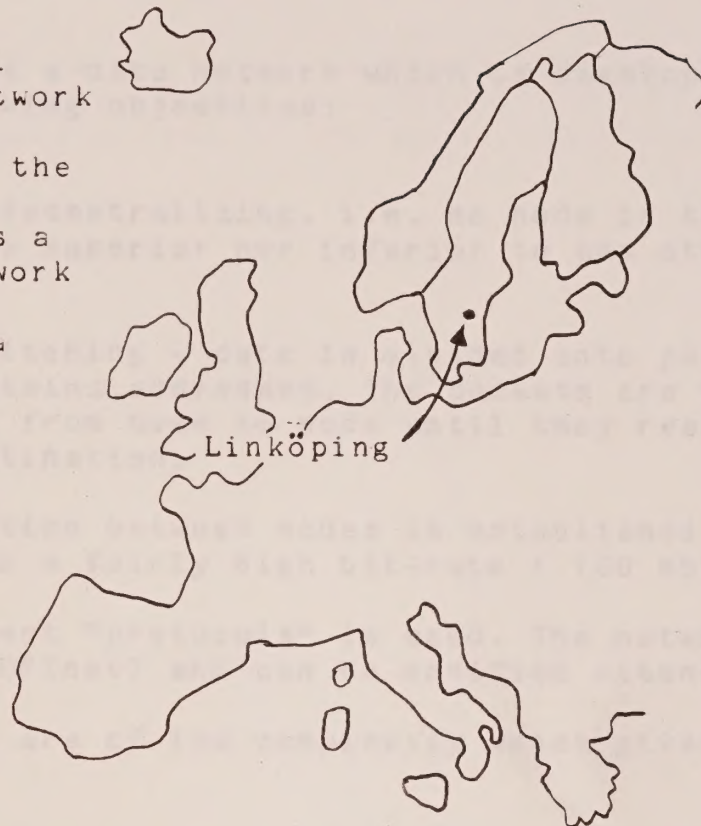


Fig 1.1 shows a typical node in this network.

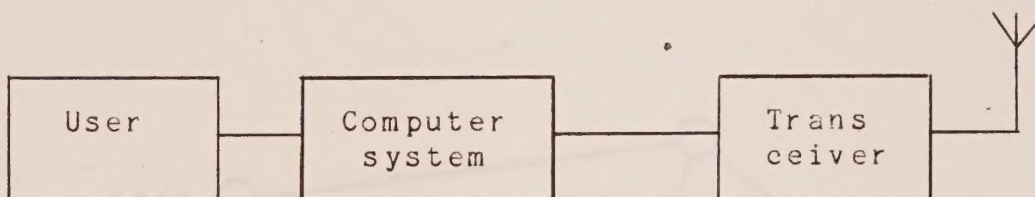


fig. 1.1 Typical node.

This report will give a short survey of the logical concepts of the network, but the main purpose is to consider the technical aspects of the microcomputer system, which is represented as a block between the user and the transceiver in the figure.

A prototype of the microcomputer system, which contains two processors with a shared memory, has been constructed and built by the authors of this report, to be used for the further development of the packet-radio network.

It is our hope that this report will be a guidance for those who later on will build their own softnet node.

1.1.1 SOFTNET, A SHORT SURVEY

Softnet is a data network which is developed with the following objectives:

- 1/ Complete decentralizing, i.e. no node in the network is superior nor inferior to any other node.
- 2/ Packet switching - data is divided into packets which contains addresses. The packets are then forwarded from node to node until they reach their destination.
- 3/ Communication between nodes is established via radio with a fairly high bit-rate (100 kbit/s).
- 4/ No permanent "protocols" is used. The network is "soft" (SOFTnet) and can be modified extensively
- 5/ The nodes are of low complexity which gives low cost.

For more detailed information see the references [1, 2].

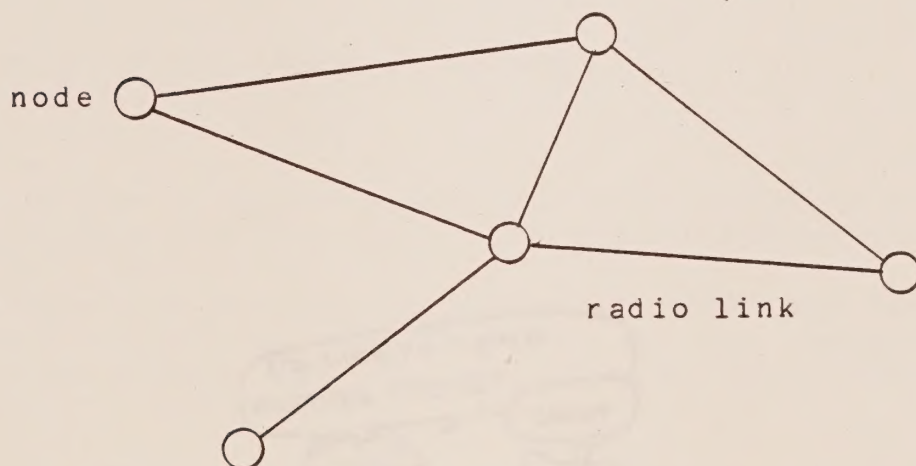


fig. 1.2 Network example.

1.1.2 THE NODE

A node can from the users point of view be seen as a port in which he plugs his terminal (or computer etc) and gets access to the whole network.

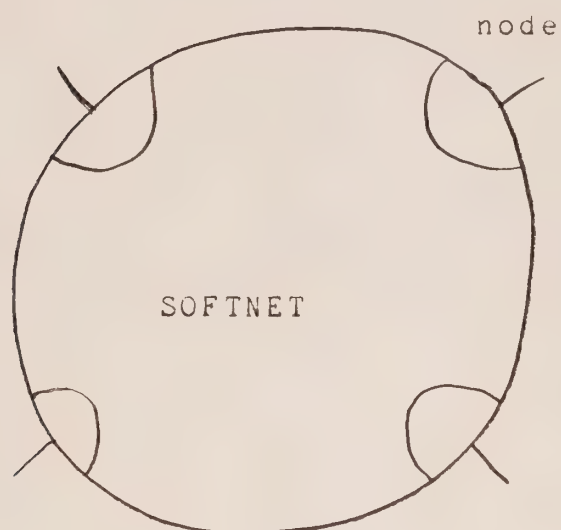


fig. 1.3 *Network structure.



The node is logically constructed as shown in figure 1.4 , where the cernel consists of the node-process, which must be a part of every node.

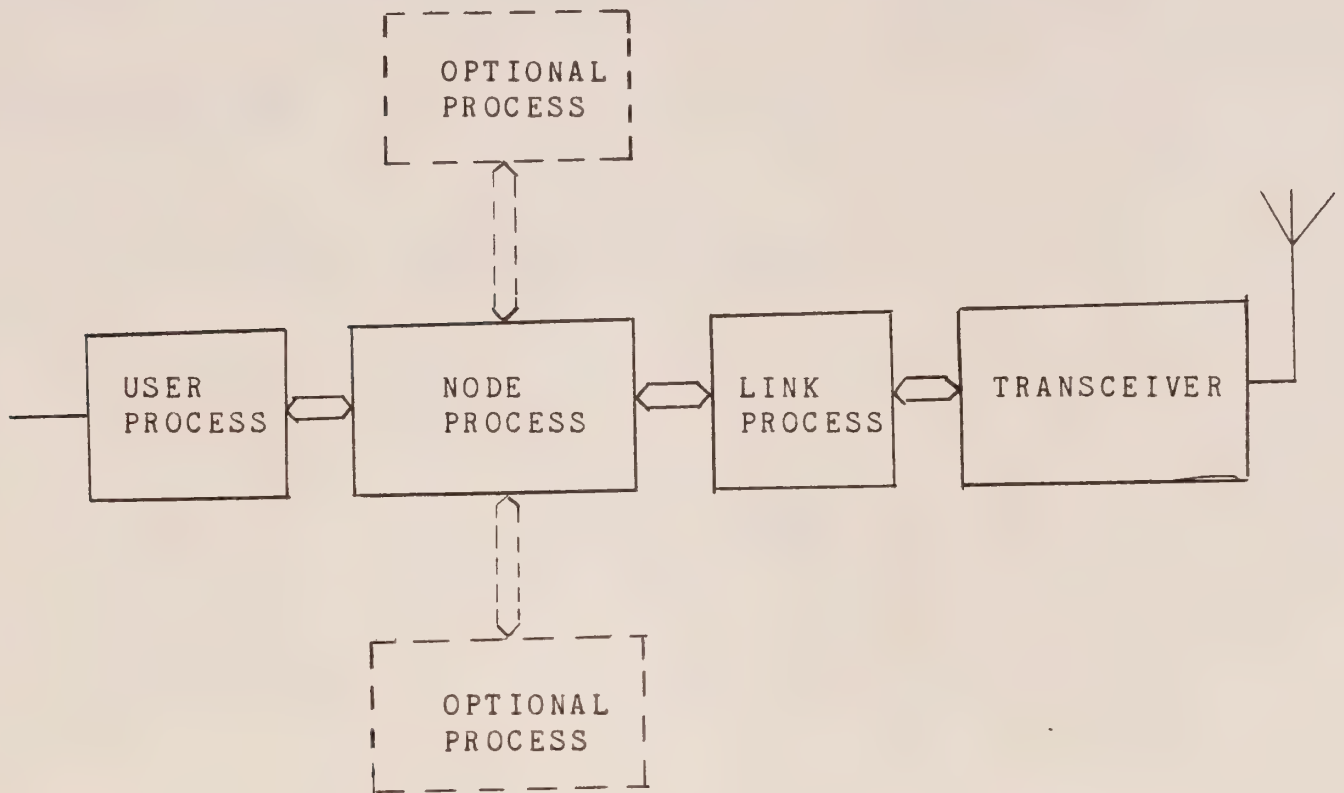


Fig. 1.4 Node processes.

It can be apprehended as a FORTH-machine that can communicate with some surrounding FORTH-processes.

The user process is the users interface towards the network and can be adapted to fulfil the users wishes. The user process transforms user data and FORTH-expressions.

The link process is the link between the node process and the transceiver.

2. SUMMARY OF THE NODE CONSTRUCTION

The node consists partly of a computer in which the necessary routing algorithms is contained and partly of a radio-part that the nodes use for communication.

2.1 TRANSCEIVER

The radio-part consists of a transmitter/receiver with the following approximative features:

- Operating frequency 450 Mhz
- Transmitter power 1 - 10 W
- Range 5 - 50 km
- Transmission rate 100 kbits/s
- Packet size 150 bytes

For further information see references [3, 4].

2.2 THE COMPUTER-PART

To accomplish the realtime demands of the link process it has its own microprocessor. The node- and user processes on the other hand do not have the same demands and therefore shares a processor. The link- and node-processes communicate via a couple of control-latches and a shared memory. See fig 2.1.

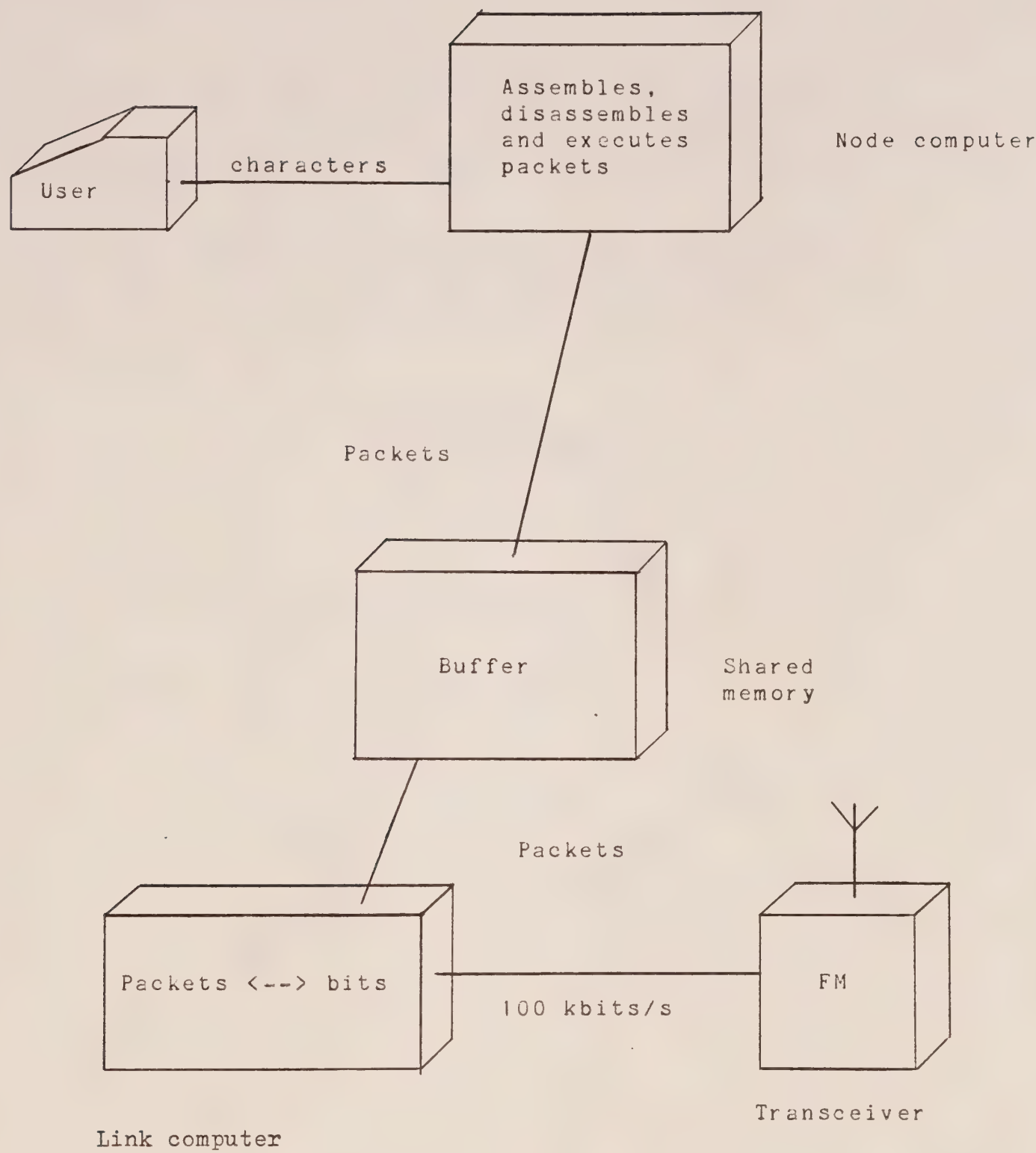


Fig. 2.1 Dataflow in a node.

2.2.1 NODE COMPUTER

The node computer is the part of the node that will be programmable by both internal and external users, and therefore will contain a large amount of RWM. Communication is performed via standard MOTOROLA peripheral circuits.

The computer is fully conventional and occupies two europe-boards. During the development phase the node computer is of trade-mark SWTPC/M6809 which is provided with a circuit board for adaption to the rest of the system.

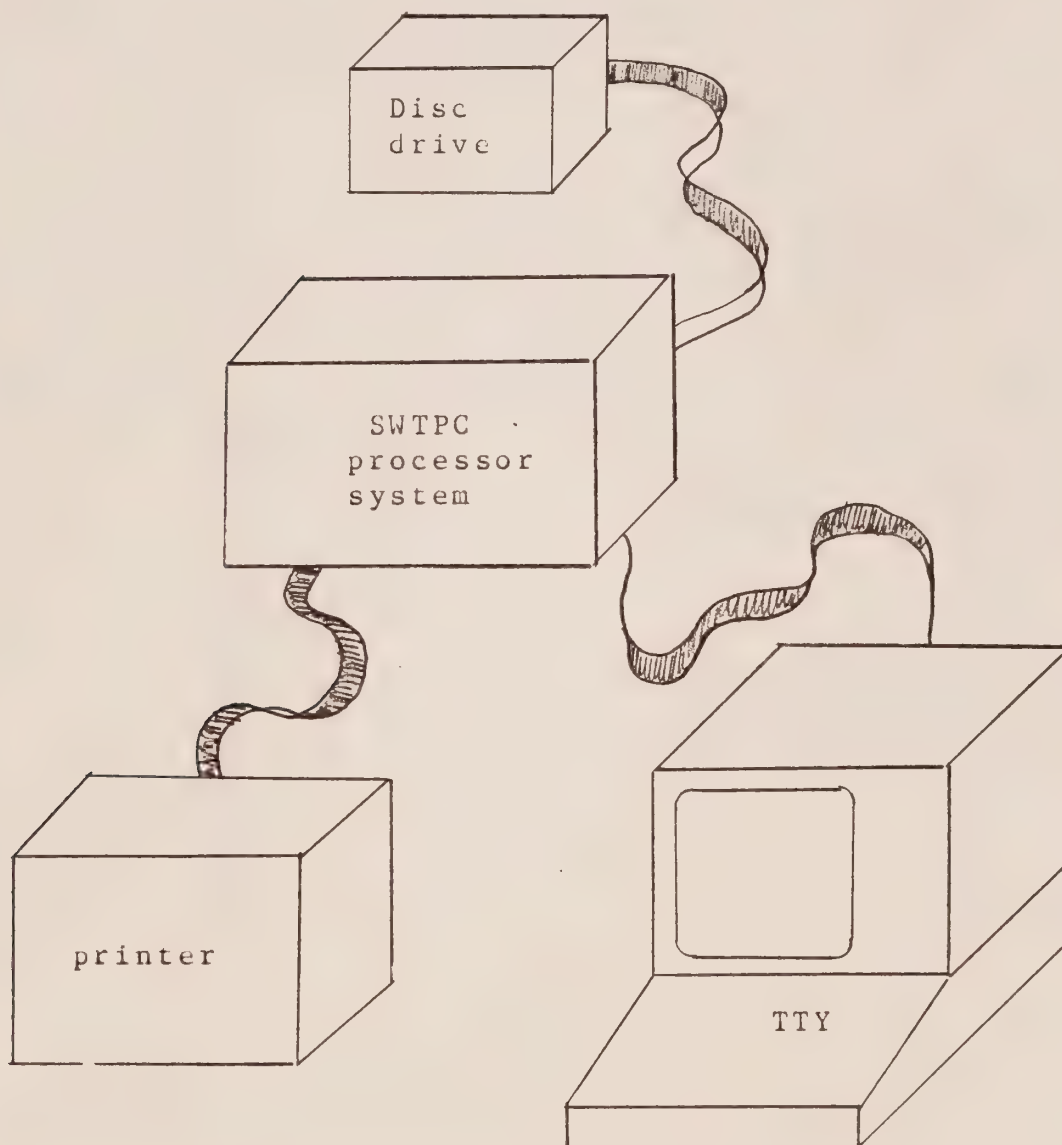


Fig. 2.2 SWTPC computer system.

Europe-board = Circuit board of size 100 * 160 mm.

2.2.2 LINK COMPUTER

Contrary to the node computer, the link computer contains a permanent set of software that is not directly accessible by the softnet users. The software will consist of programs for control of addresses checksums etc, access algorithms and collection of data for statistical computations. The link computer is fully controlled through the control-latches and the shared memory.

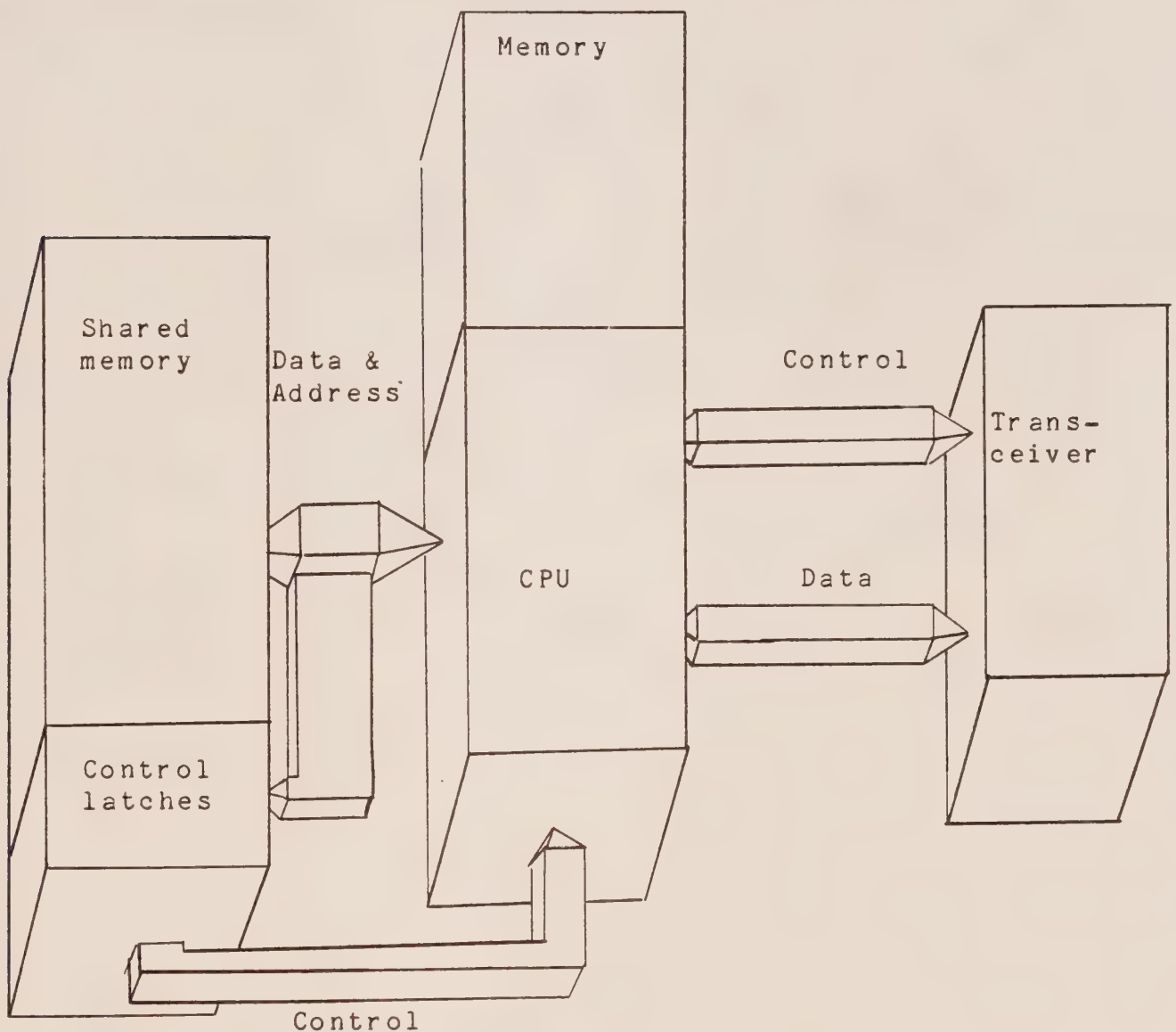


Fig. 2.3 Link computer.

2.2.3 THE SHARED MEMORY AND CONTROL LATCHES

The shared memory is the main feature in the two-processor system and is the channel by which the two processors communicate.

From the hardware point of view it is built to allow both processors to access the memory independently.

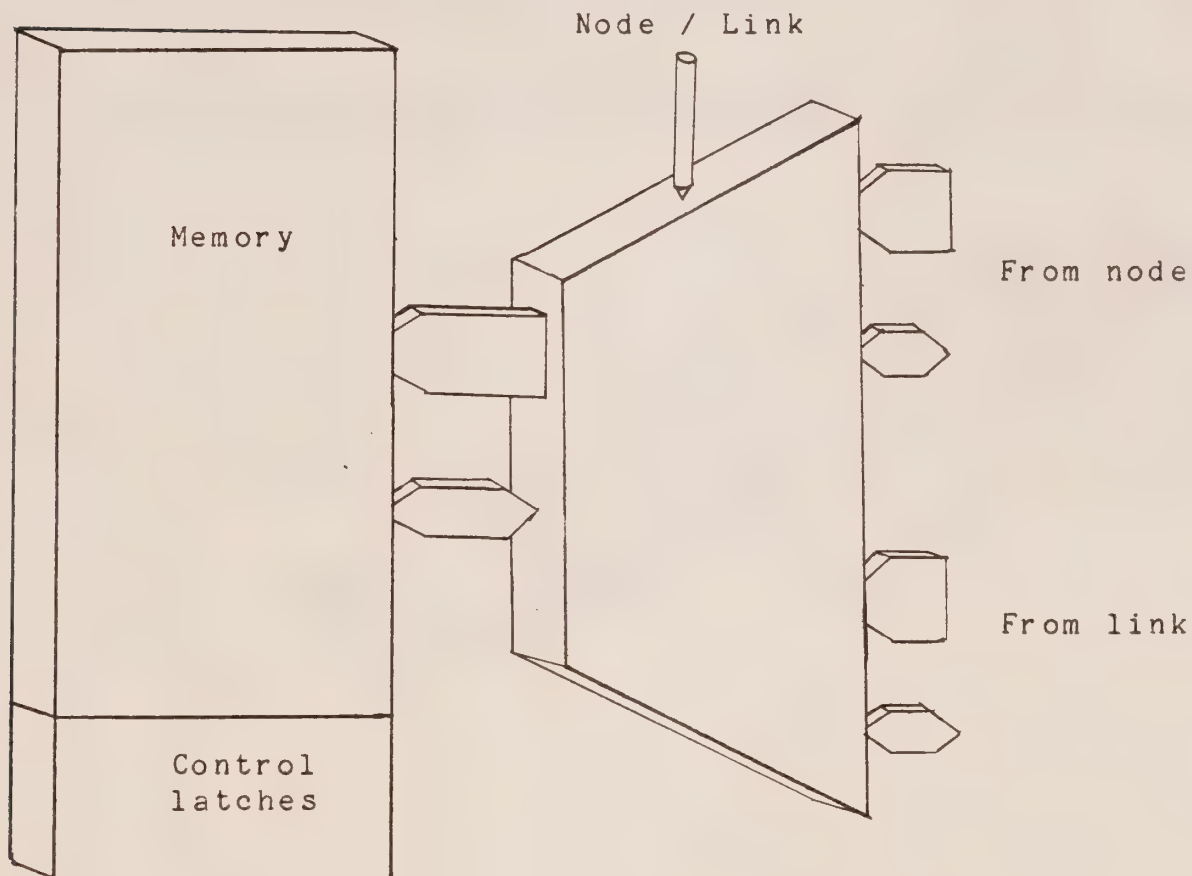


Fig. 2.4 Shared memory.

3. NODE CONSTRUCTION

The construction is built around the Motorola M6809 microprocessor. Some reasons for the choice of this processor are these:

- Suitable for FORTH-implementation.
- Suitable for shared memory.
- Sound programming structure.

For easy interchanging of memorytypes, memorys of byte-wide type has been chosen (RWM, PROM).



3.1 PHYSICAL DEVICE CONSTRUCTION

The circuit boards that constitutes the system are put into a 19" rack, and connected through a common bus. In the prototype system the SWTPC computer is used as the node computer. It is connected via a specially made interface board.

3.2 BUSES AND CIRCUIT BOARDS

The 96 bit bus can be regarded as three 32 bit buses (A, B and C).

A: The node computer's address- and data-bus.

B: Link - transceiver interface.

C: Supply voltages and control signals.

Furthermore, there is an "internal" bus for connection of the link computer's circuit boards.

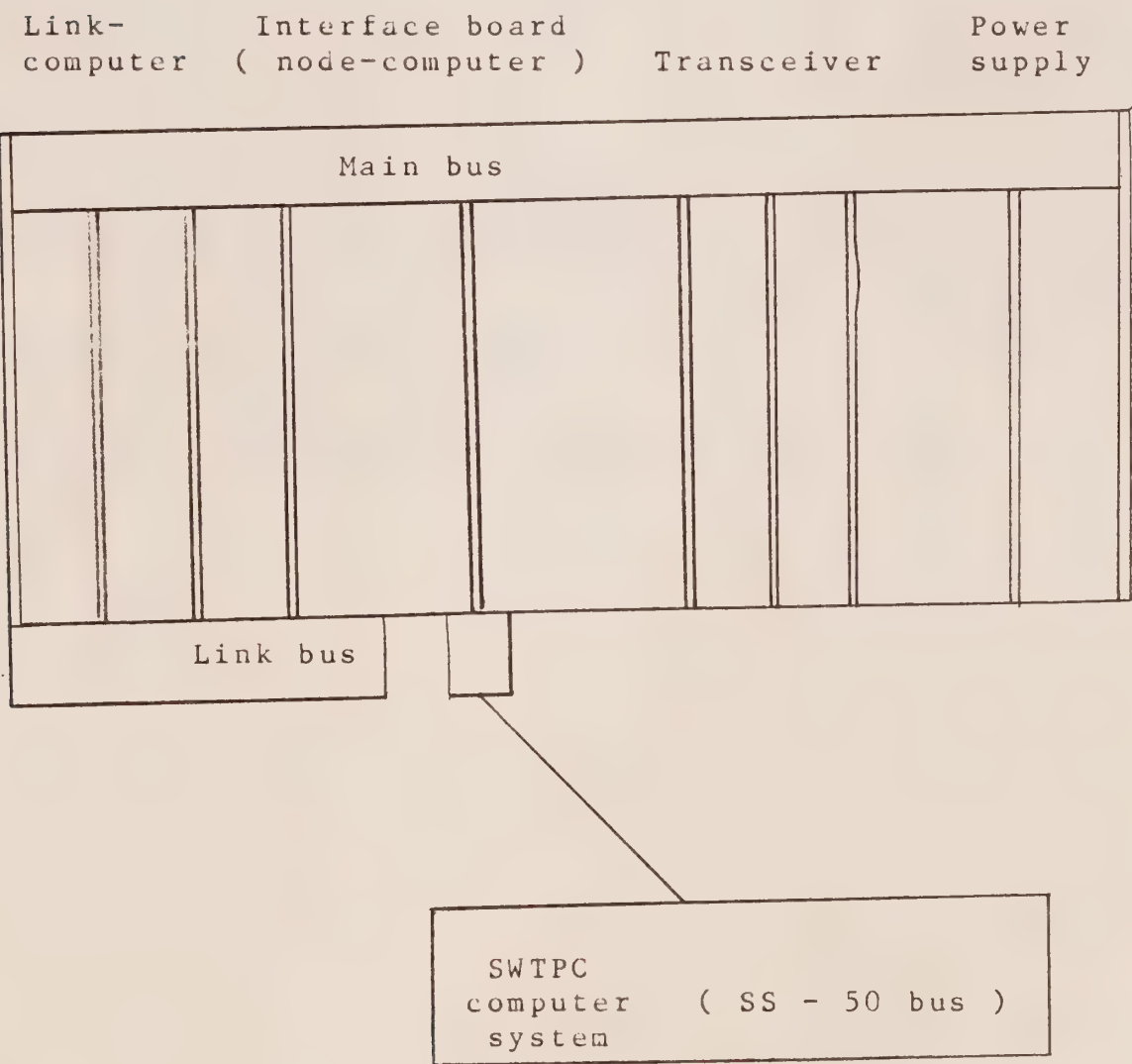


Fig. 3.1 Bus structure.

3.3 NODE COMPUTER

As was earlier pointed out, the node computer is a conventional microcomputer with a large memory. It occupies two circuit boards.

- 1/ CPU board: Besides the M6809 processor it also contains
 - PROM with necessary software,
 - terminal communication (ACIA),
 - watchdog, i.e. a circuit that restores the computer when errors arises.

- 2/ Memory board: 64 kbyte.

3.3.1 SWTPC SYSTEM

To accomplish easy and efficient program-development, a complete computer system is used as node computer.

The chosen system contains several software-tools, such as editor, assembler etc.

The computer also contains PROM-writer, discettes etc, which are useful in a prototype.

3.3.2 INTERFACE BOARD TO SWTPC

The interface board is for adaption of the SWTPC's SS-50 bus to the 96 bit bus that is a part of the specific hardware.

Furthermore the 5 higher bits of the address bits are decoded and gives bus signals for the shared memory, and one for the control latches.

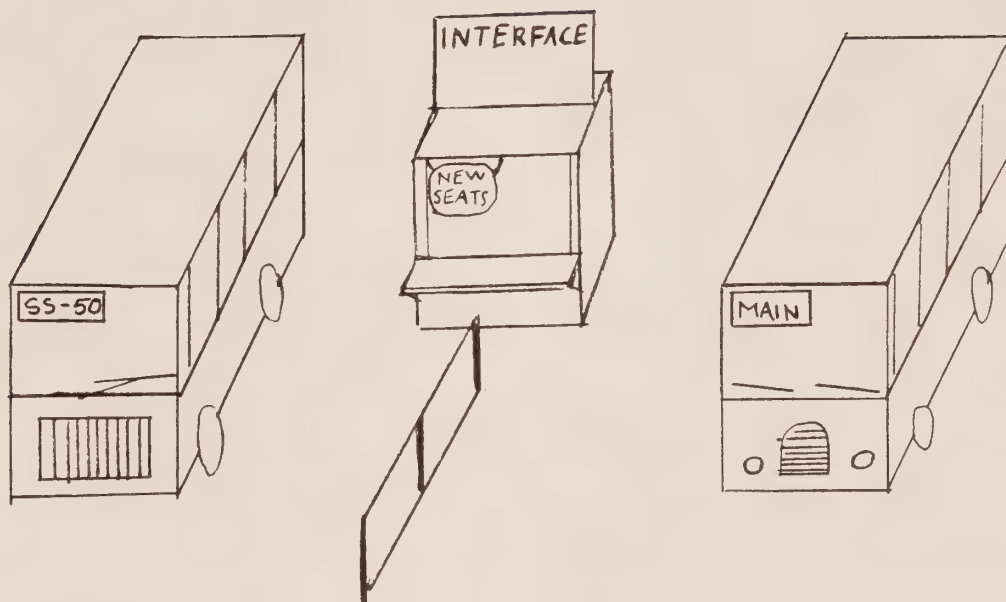


Fig. 3.2 Interface board.

SS - 50 BUS

MAIN BUS

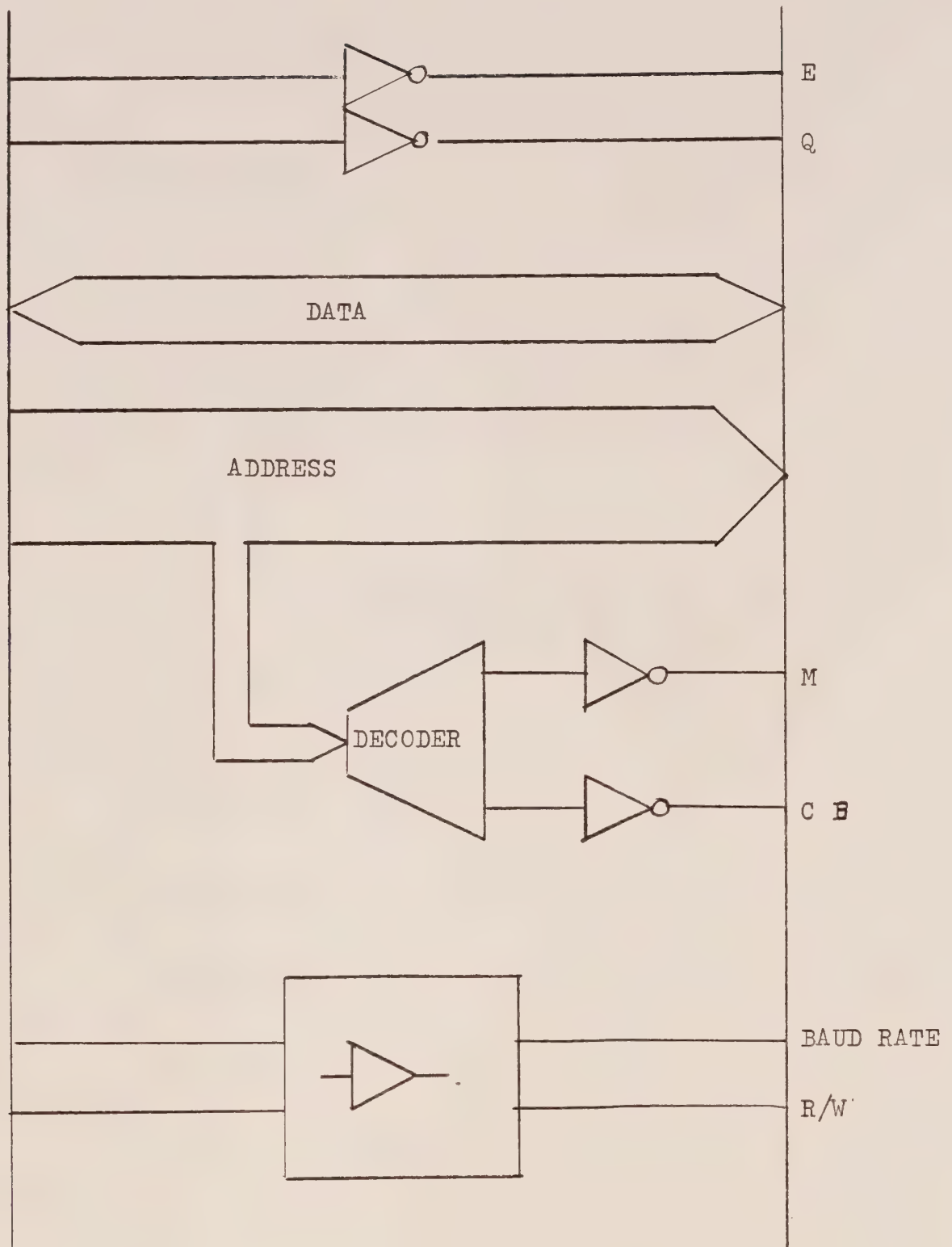


Fig 3.3 Interface.

3.4 SHARED MEMORY BOARD

3.4.1 CONTROL LATCHES

The control latches consists of 8 D-type latches that can be addressed, read and written like a common memory byte. Their function is to control the link processor and to control the node processors addressing of the shared memory.

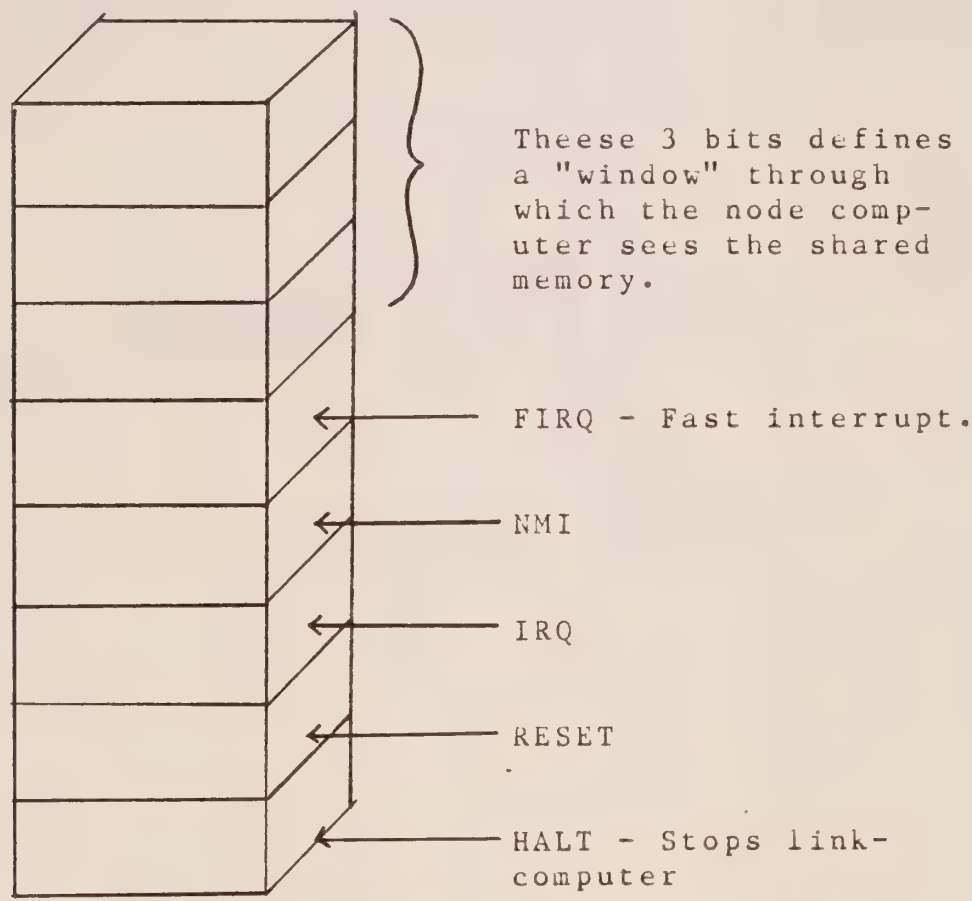


Fig. 3.4 Control latches.

The control "byte" can be regarded as a part of the shared memory, but is always accessible from both processors.

3.4.2 SHARED MEMORY

To make a fast transfer of data and program between the node- and link computer possible, the lower 16 kbyte of the link computer are also accessible from the node computer.

The node computer "sees" this memory through a 2 kbyte wide "window", that can be moved by the control-latches.

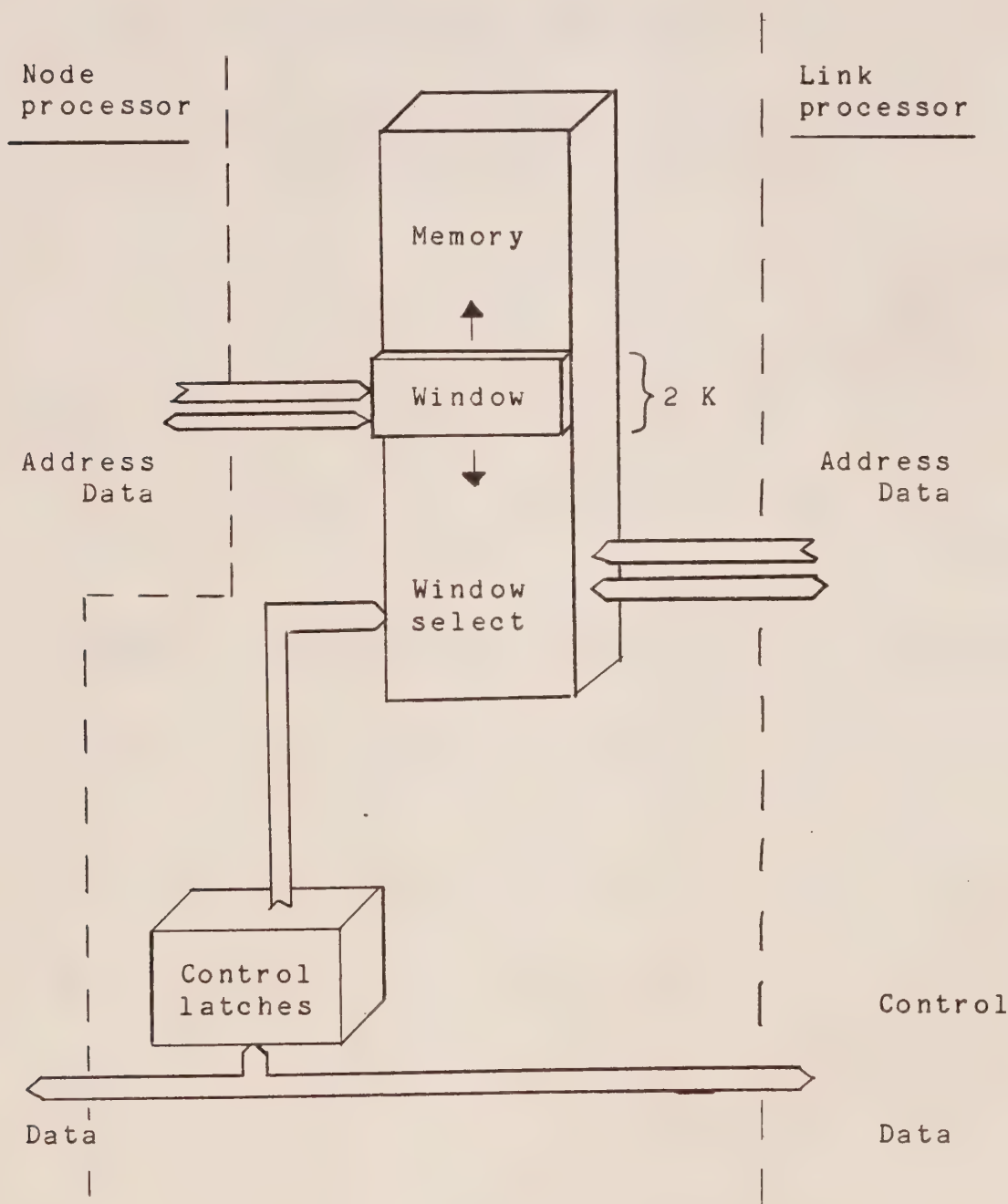


Fig. 3.5 Shared memory.

3.4.3 FUNCTION DESCRIPTION

In order to make the memory accessible from two processors simultaneously, some kind of time-sharing is necessary.

This time-sharing is carried out so that each processor only gets access to the memory during half the clock-cycle. For that reason the link-processor's clock is delayed half a cycle.

For switching address and databuses to the memory, tri-state buffers are used.

A complete timing-diagram for the memory is shown below. You can also see that the memory has to be fast to meet the demands (< 350 ns).

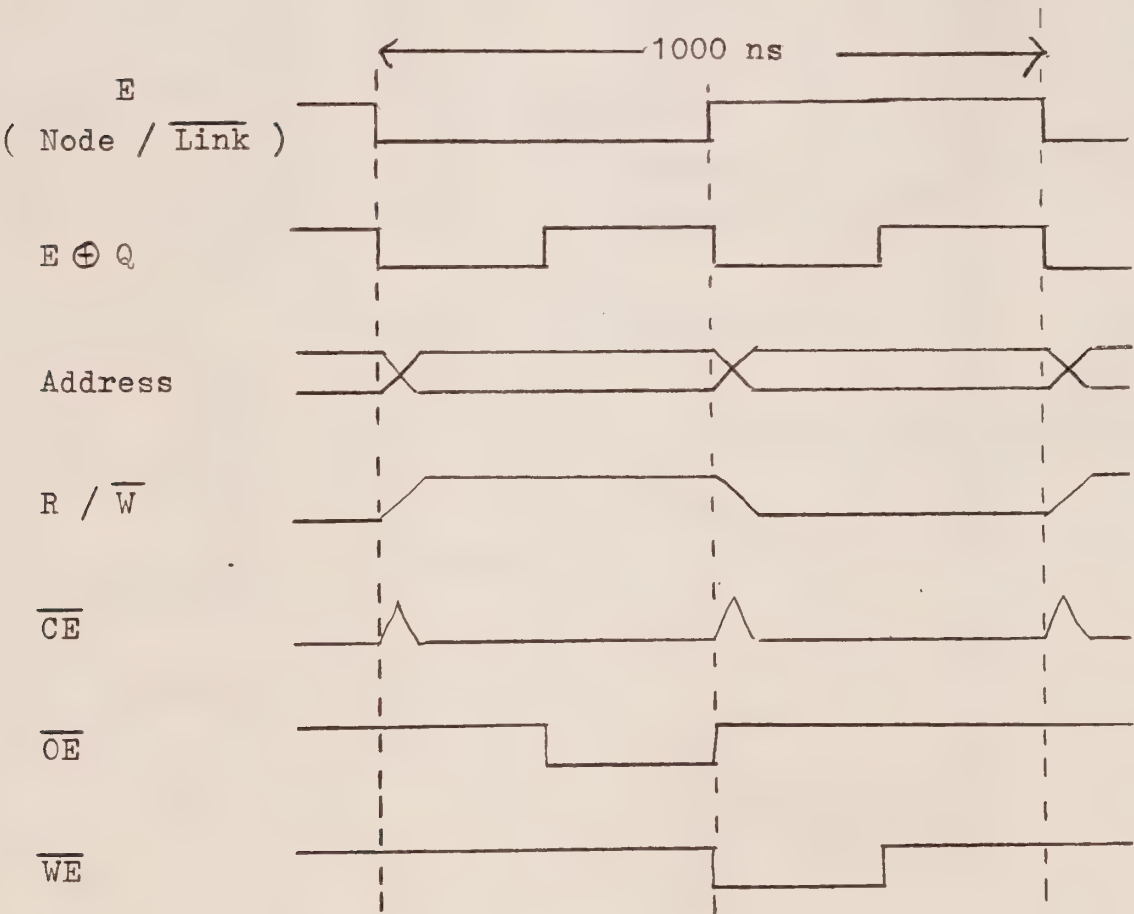


Fig . 3.6 Timing diagram.

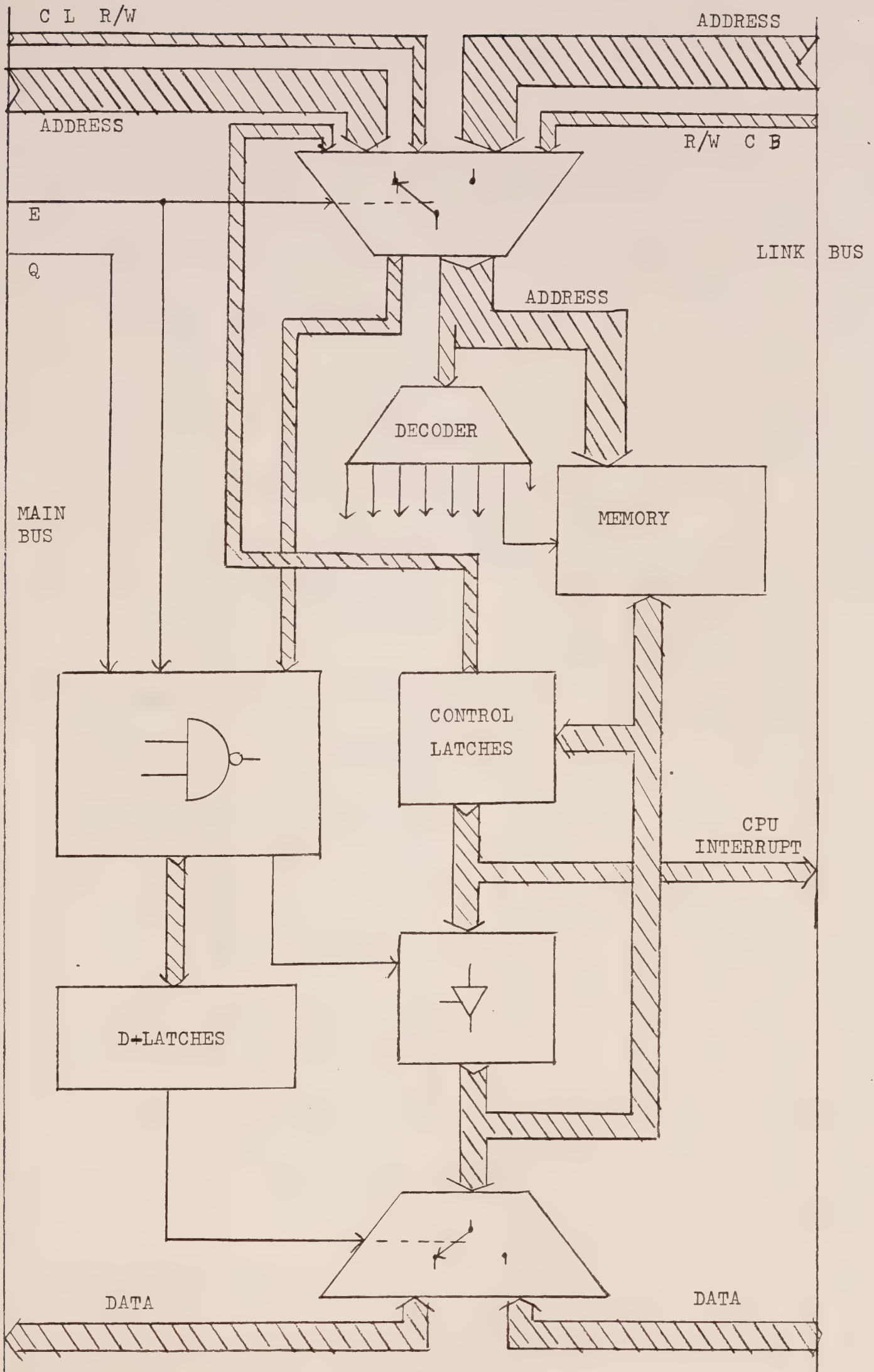


Fig. 3.7 Shared memory.

3.5 LINK COMPUTER

The link computer has rather well-specified and limited tasks, and is not intended for on-line programming by users. For this reason it will not need large amounts of memory.

The computer is built on two circuit boards containing:

- CPU and the top memory.
- I/O and memory.

The I/O can be divided into:

- serial I/O for data to / from transceiver,
- parallel I/O for control signals,
- serial tty communication. (Prototype only.)

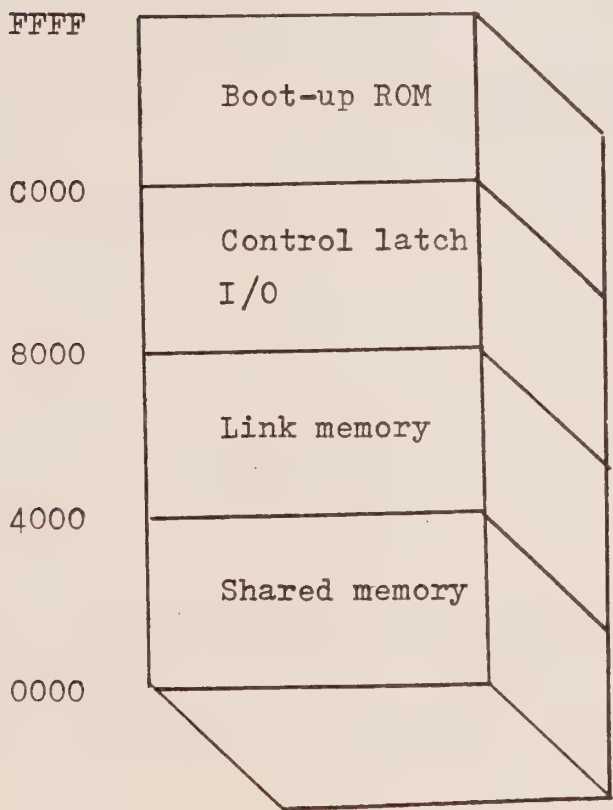


Fig. 3.8 Link memory.

3.5.1 CPU

The link computer contains a Motorola M6809E. The E-type makes use of an external clocksignal which allows it to use the clock generated by the node processor.

Synchronisation of the processors is necessary in order to share the same memory.

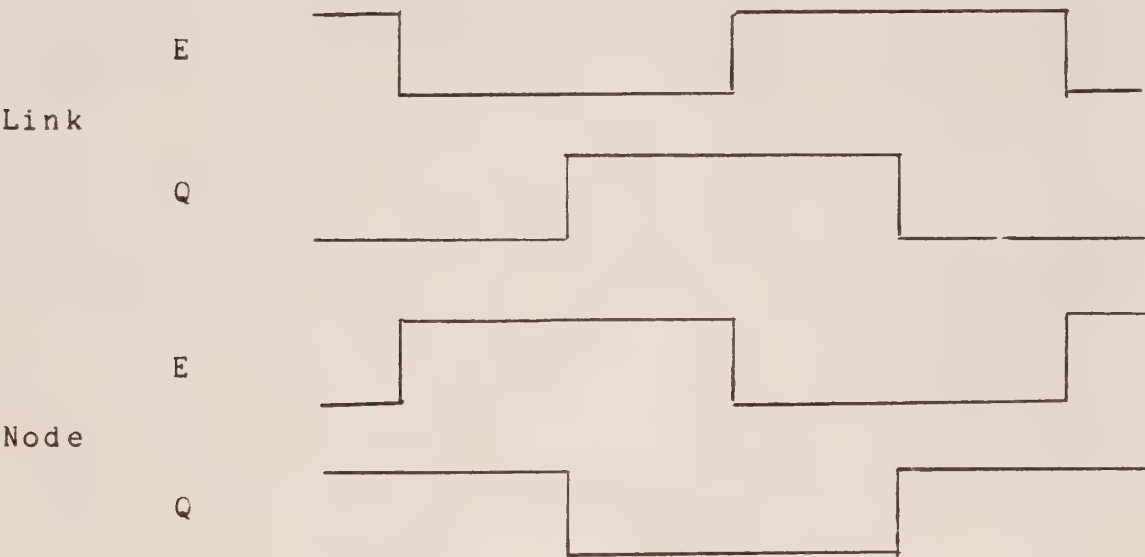


Fig. 3.10 MPU clocks.

3.5.2 MEMORY

To simplify memory modifications, byte-wide chips (Mostek, 2 kbyte) are used.

A timing diagram is shown in figure 3.11.

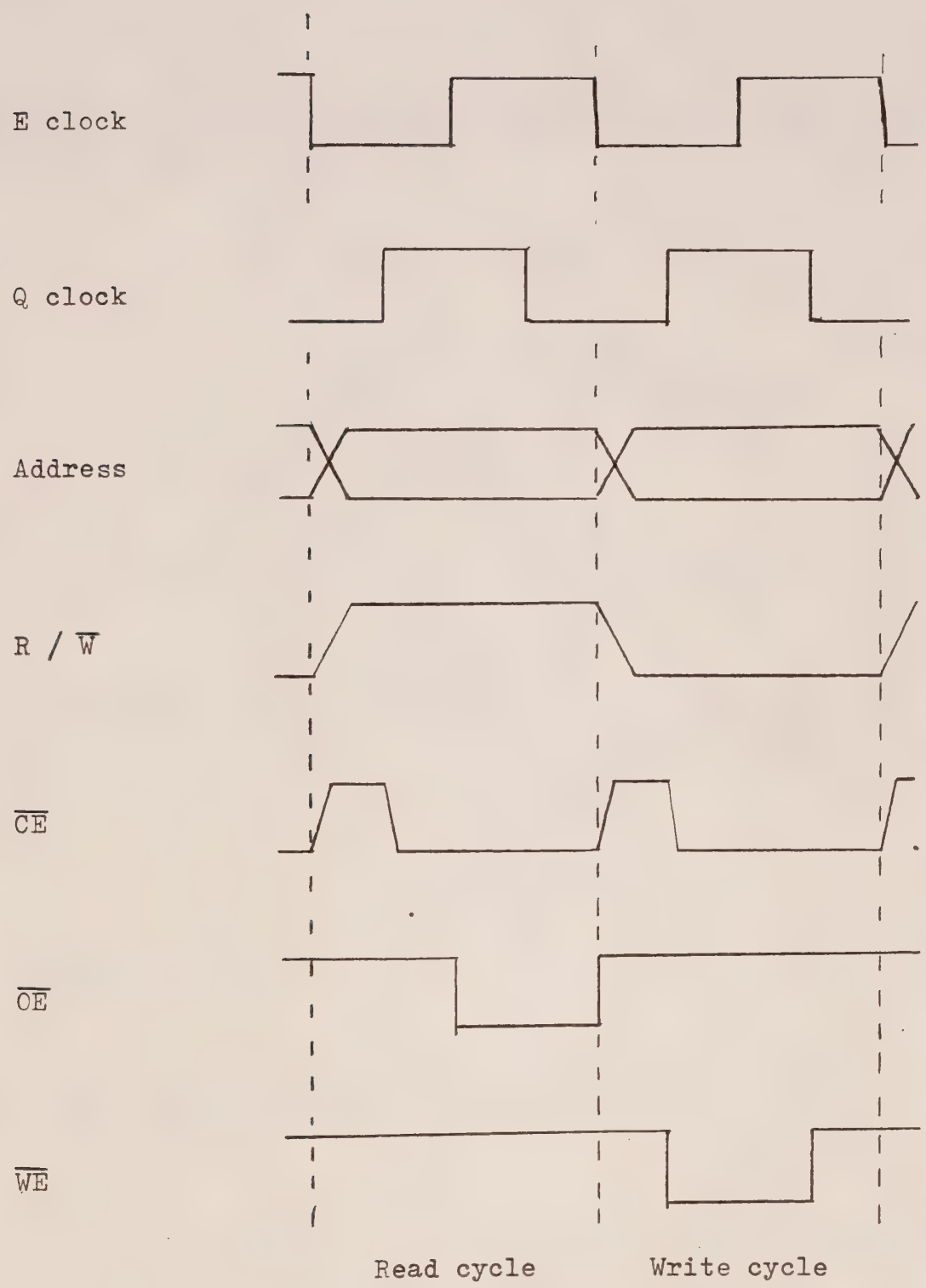


Fig. 3.11 Memory timing

3.5.3

I/O

The I/O consists of communication with the transceiver. It uses synchronous, serial data transmission and parallel control signals.

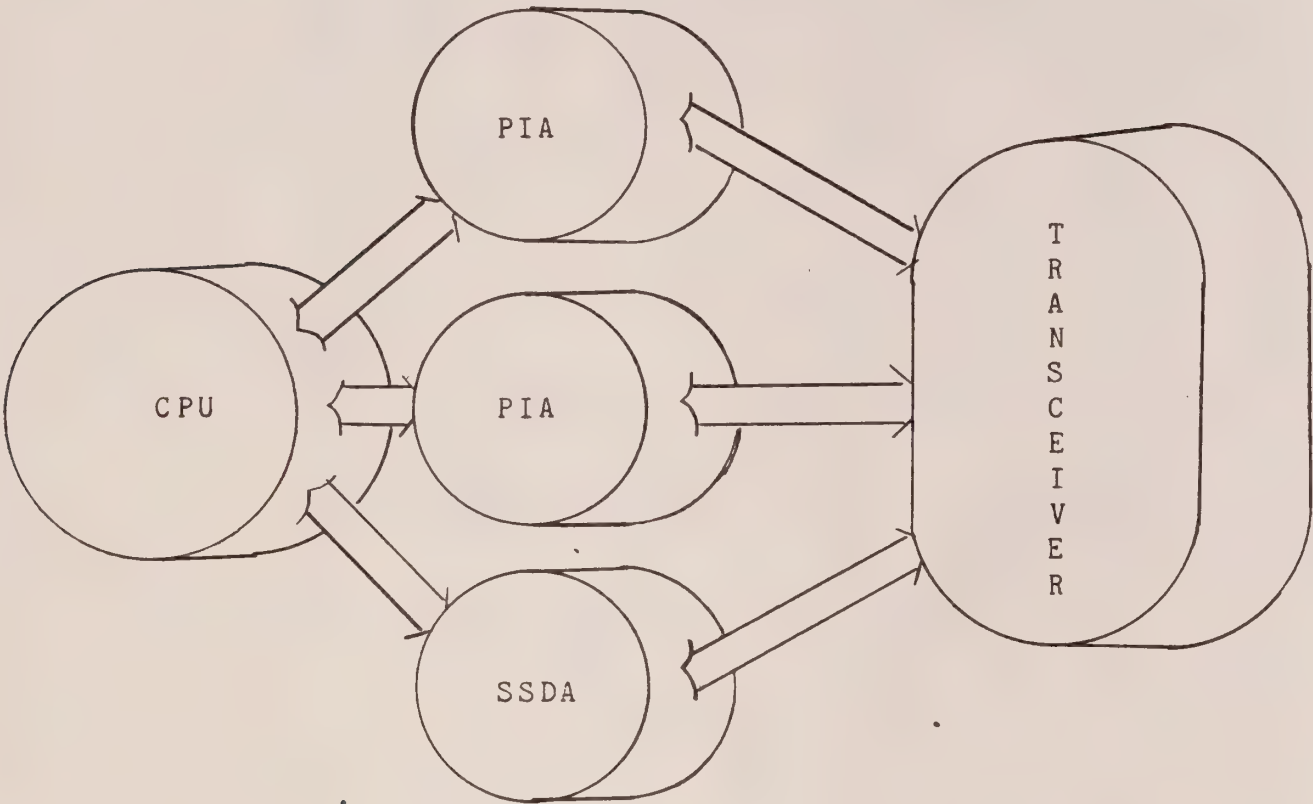


Fig. 3.12

To simplify debugging, the prototype is also equipped with a serial tty port.

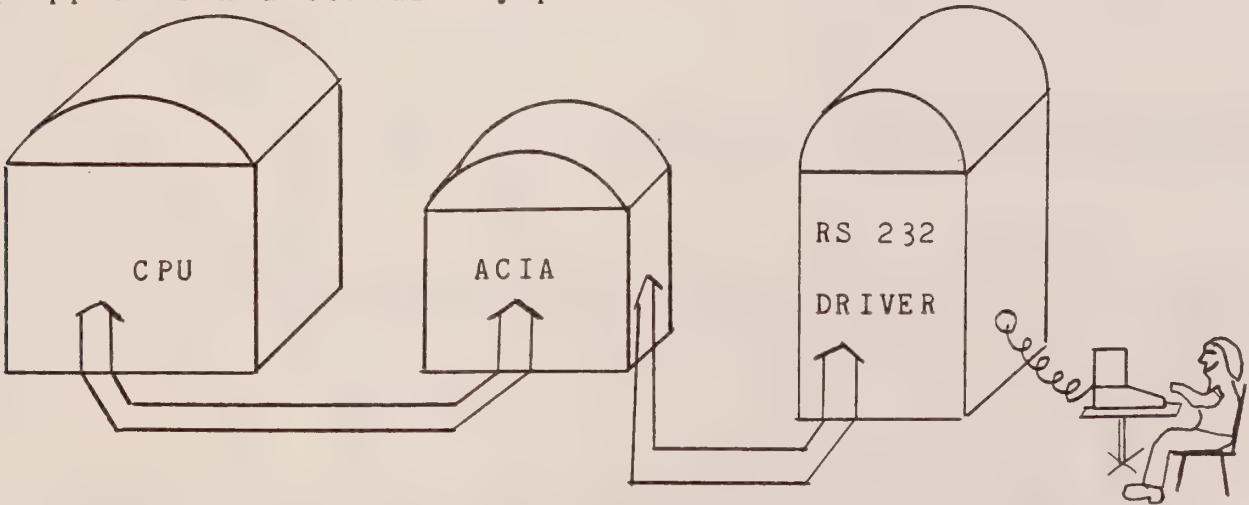


Fig. 3.13 TTY port.

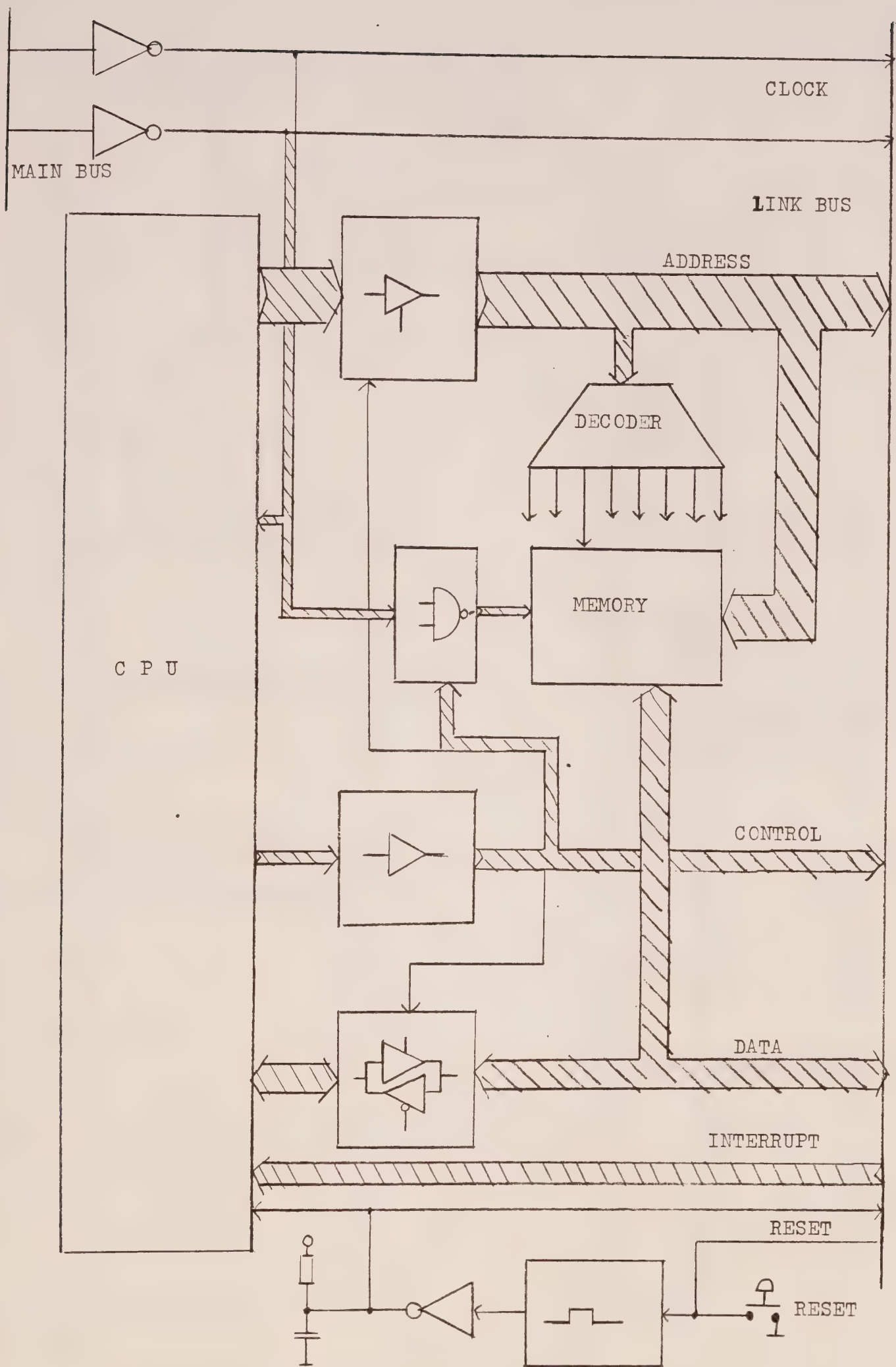


Fig 3.14 Link CPU.

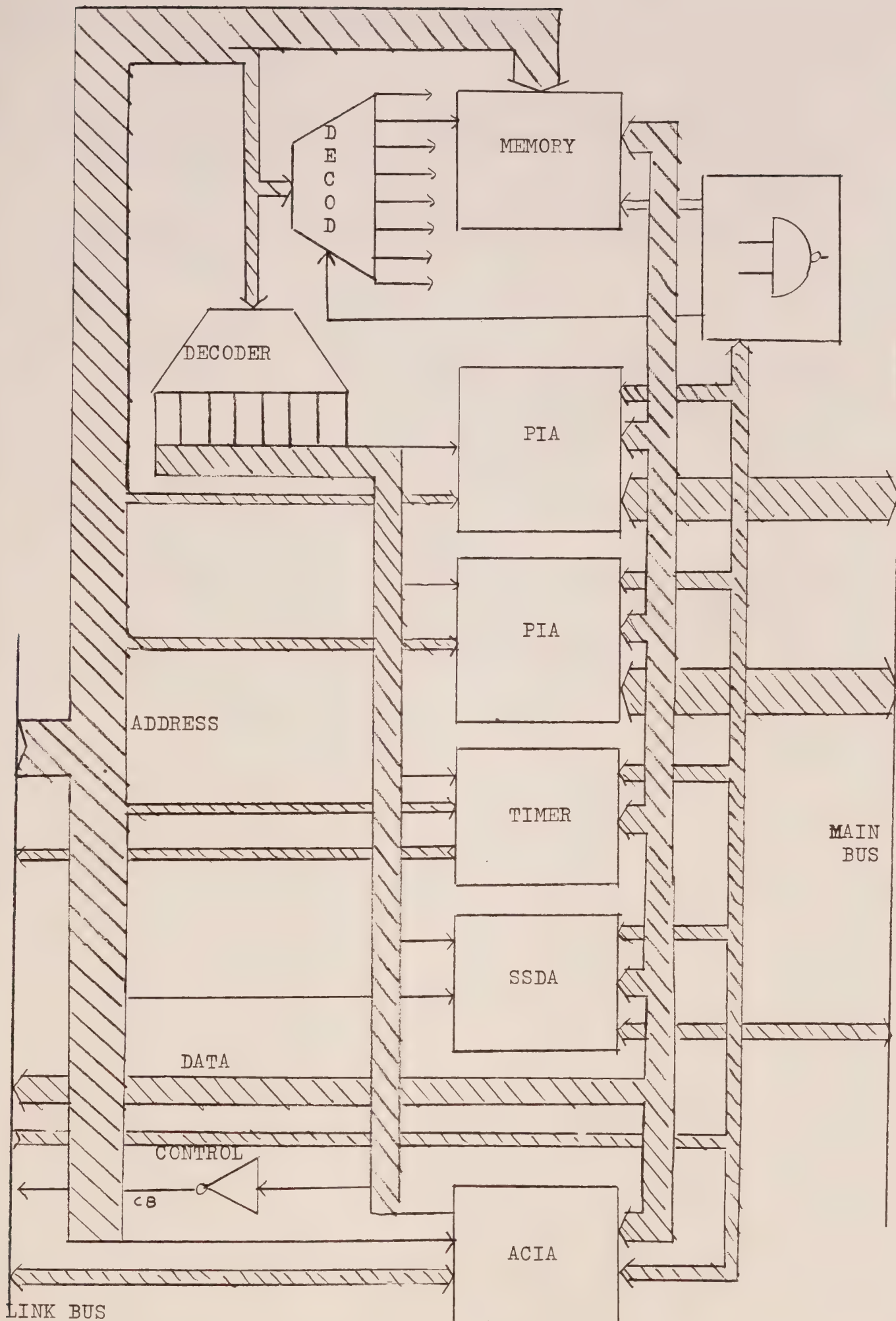


Fig. 3.15 Link I/O.

3.5.5

PROTOTYPE SOFTWARE

Besides some initialisation programs for the I/O circuits, the link computer contains a very simple monitor for the tty-line.

This monitor can be used for displaying and modification of the memory contents, and for program execution.

Command:

M nnnn

Display contents of memory-word
on address nnnn (hex).

Contents may be changed
by typing the new value.

↑

Previous word.

↓

Next word.

P nnnn

Start execute from address nnnn.

G

Start execute from the latest
typed address.

REFERENCES

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"Design considerations of a distributed
packet radio network using the radio
amateur band".
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- 2 Zander, J., Forchheimer, R. :
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computer- and radio-amateurs".
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- 3 Skoglund, M., Persson, P-M. :
"Construction of a packet-radio modem".
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- 4 Galli, P :
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- 5 Motorola inc.
"MC6809 - MC6809E microprocessor
programming manual".

A1 CPU, I/O AND MEMORY CIRCUITS

A1.1 M 6809 CPU

**MOTOROLA****Product Preview****HIGH-PERFORMANCE MICROPROCESSOR**■ **MC6800 COMPATIBLE**

- Hardware — Interfaces With All M6800 Peripherals
- Software — Upward Compatible Instruction Set and Addressing Modes

■ **HARDWARE FEATURES**

- On-Chip Oscillator (MC6809) 4 X to Clock
- Optional ± 1 External Clock Inputs (MC6809E)
- MRDY Input Extends Data Access Times for Use With Slow Memory
- BREQ/TSC Allows Quick Access to Bus for DMA and Memory Refresh
- Last Instruction Cycle Output for Identification of Opcode Fetch (MC6809E)
- Fast Interrupt Request Input Stacks Only Program Counter and Condition Code
- Interrupt Acknowledge Output Allows Vectoring by Device
- Busy Output Eases Multiprocessor Design (MC6809E)

■ **ARCHITECTURAL FEATURES**

- Two 8-Bit Accumulators Can Be Concatenated to Form One 16-Bit Accumulator
- Two 16-Bit Index Registers
- Two 16-Bit Indexable Stack Pointers
- Direct Page Register Allows Direct Addressing Throughout Memory Space

■ **INSTRUCTION SET**

- Extended Range Branches
- 16-Bit Arithmetic
- Push/Pull Any Register or Set of Registers To/From Either Stack
- 8 X 8 Unsigned Multiply
- Transfer/Exchange Any Two Registers of Equal Size
- Enhanced Pointer Register Manipulation

■ **ADDRESSING MODES**

- All MC6800 Modes, Plus PC Relative, Extended Indirect, Indexed Indirect, and PC Relative Indirect
- Direct Addressing Available for All Memory Access Instructions
- Index Mode Options Include Accumulator or Up to 16-Bit Constant Offset, and Auto-Increment/Decrement (by 1 or 2) With Any of the Four Pointer Registers

MC6809(E)

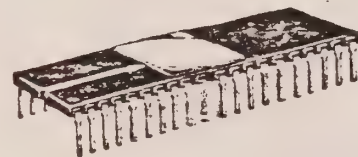
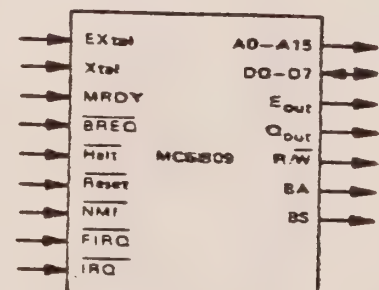
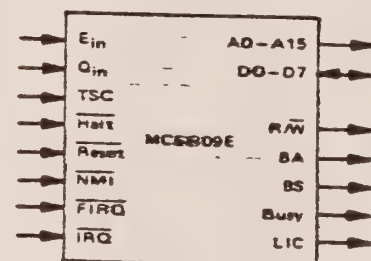
(1.0 MHz)

MC68A09(E)

(1.5 MHz)

MC68B09(E)

(2.0 MHz)

MOS(N-CHANNEL SILICON-GATE,
DEPLETION LOAD)**HIGH-PERFORMANCE
MICROPROCESSOR****L SUFFIX
CERAMIC PACKAGE
CASE 715****NOT SHOWN:
P SUFFIX
PLASTIC PACKAGE
CASE 711****FIGURE 1 — BLOCK DIAGRAMS**

This is advance information and specifications are subject to change without notice.

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NP-98 R1

A1.2 M 6821 PIA



MOTOROLA

PERIPHERAL INTERFACE ADAPTER (PIA)

The MC6821 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the MC6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines
- Two TTL Drive Capability on All A and B Side Buffers
- TTL-Compatible
- Static Operation

ORDERING INFORMATION

Speed	Device	Temperature Range
1.0 MHz	MC6821P, L	0 to +70°C
	MC6821CP, CL	-40 to +85°C
MIL-STD-883B MIL-STD-883C	MC6821BQCS MC6821CQCS	-55 to +125°C
1.5 MHz	MC68A21P, L	0 to +70°C
	MC68A21CP, CL	-40 to +85°C
2.0 MHz	MC68B21P, L	0 to +70°C

MC6821
(1.0 MHz)

MC68A21
(1.5 MHz)

MC68B21
(2.0 MHz)

MOS

(IN-CHANNEL, SILICON-GATE,
DEPLETION LOAD)

PERIPHERAL INTERFACE
ADAPTER



L SUFFIX
CERAMIC PACKAGE
CASE 715



P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN ASSIGNMENT

1	O	CA1	40
2	VSS	CA2	39
3	PA0	PROA	38
4	PA1	PROB	37
5	PA2	RS0	36
6	PA3	RS1	35
7	PA4	PROB	34
8	PA5	DO	33
9	PA6	D1	32
10	PA7	D2	31
11	PB0	D3	30
12	PB1	D4	29
13	PB2	D5	28
14	PB3	D6	27
15	PB4	D7	26
16	PB5	E	25
17	PB6	CS1	24
18	PB7	CS2	23
19	CB1	CS0	22
20	CB2	R/W	21

A1.3 M 6840 TIMER



MC6840
MC68A40
MC68B40

PROGRAMMABLE TIMER MODULE (PTM)

The MC6840 is a programmable subsystem component of the M6800 family designed to provide variable system time intervals.

The MC6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The MC6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

- Operates from a Single 5 Volt Power Supply
- Fully TTL Compatible
- Single System Clock Required (Enable)
- Selectable Prescaler on Timer 3 Capable of 4 MHz for the M6840, 6 MHz for the MC68A40 and 8 MHz for the MC68B40
- Programmable Interrupts ($\overline{TRQ}$) Output to MPU
- Readable Down Counter Indicates Counts to Go to Time-Out
- Selectable Gating for Frequency or Pulse-Width Comparison
- RESET Input
- Three Asynchronous External Clock and Gate/Trigger Inputs Internally Synchronized
- Three Maskable Outputs

MOS
(N-CHANNEL, SILICON-GATE
DEPLETION LOAD)
PROGRAMMABLE TIMER

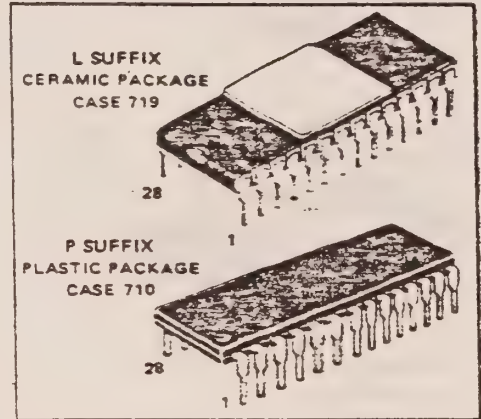
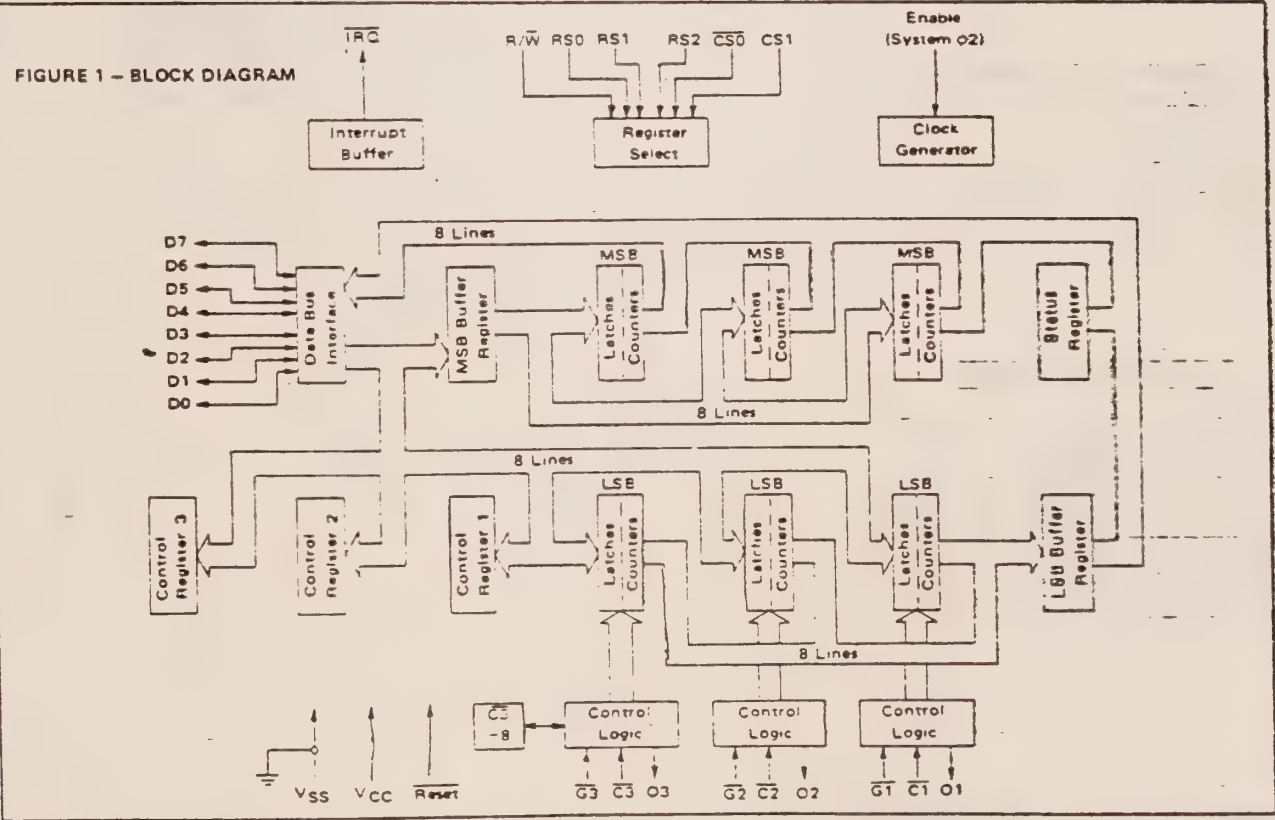


FIGURE 1 - BLOCK DIAGRAM



A1.4 M 6850 ACIA



MC6850
1.0 MHz
MC68A50
1.5 MHz
MC68B50
2.0 MHz

ASYNCHRONOUS COMMUNICATIONS INTERFACE
ADAPTER (ACIA)

The MC6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the MC6800 Microprocessing Unit.

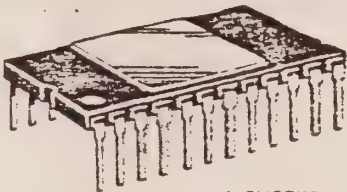
The bus interface of the MC6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation three control lines are provided. These lines allow the ACIA to interface directly with the MC6860L 0-600 bps digital modem.

- Eight and Nine-Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional $\div 1$, $\div 16$, and $\div 64$ Clock Modes
- Up to 500 kbps Transmission
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered
- One or Two Stop Bit Operation

MOS

(IN-CHANNEL SILICON-GATE)

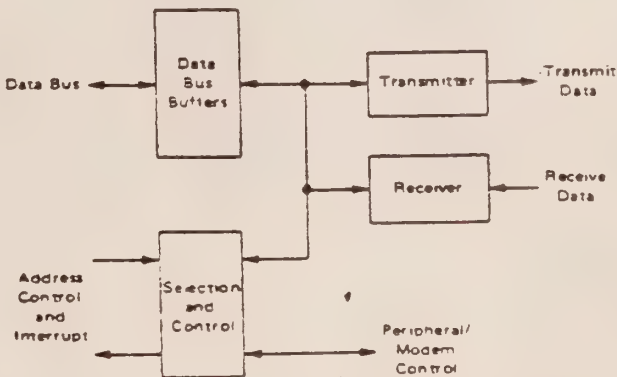
ASYNCHRONOUS
COMMUNICATIONS INTERFACE
ADAPTER



L SUFFIX
CERAMIC PACKAGE
CASE 716

NOT SHOWN: P SUFFIX
PLASTIC PACKAGE
CASE 709

MC6850 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER
BLOCK DIAGRAM



ORDERING INFORMATION

Speed	Device	Temperature Range
1.0 MHz	MC6850P,L	0 to +70°C
	MC6850CP,CL	-40 to +85°C
MIL-STD-883B	MC6850BJCS	-55 to +125°C
MIL-STD-883C	MC6850CJCS	
1.5 MHz	MC68A50P,L	0 to +70°C
	MC68A50CP,CL	-40 to +85°C
2.0 MHz	MC68B50P,L	0 to +70°C

A1.5 M 6852 SSDA



SYNCHRONOUS SERIAL DATA ADAPTER (SSDA)

The MC6852 Synchronous Serial Data Adapter provides a bi-directional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the M6800 Microprocessor systems.

The bus interface of the MC6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization. Programmable control registers provide control for variable word lengths, transmit control, receive control, synchronization control, and interrupt control. Status, timing and control lines provide peripheral or modem control.

Typical applications include floppy disk controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

- Programmable Interrupts from Transmitter, Receiver, and Error Detection Logic
- Character Synchronization on One or Two Sync Codes
- External Synchronization Available for Parallel-Serial Operation
- Programmable Sync Code Register
- Up to 600 kbps Transmission
- Peripheral/Modem Control Functions
- Three Bytes of FIFO Buffering on Both Transmit and Receive
- Seven, Eight, or Nine Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun, and Underflow Status

MC6852
(1.0 MHz)

MC68A52
(1.5 MHz)

MC68B52
(2.0 MHz)

MOS
(N-CANNEL, SILICON GATE)

SYNCHRONOUS
SERIAL DATA
ADAPTER



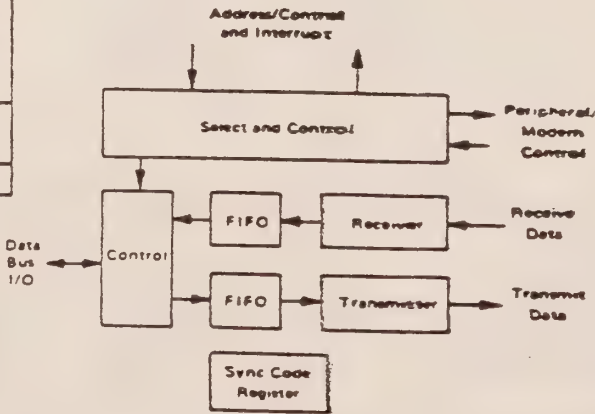
L SUFFIX
CERAMIC PACKAGE
CASE 716

NOT SHOWN: P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

Speed	Device	Temperature Range
1.0 MHz	MC6852P,L	0 to +70°C
	MC6852CP,CL	-40 to +85°C
	MC6852BJCS	-55 to +125°C
	MC6852CJCS	
1.5 MHz	MC68A52P,L	0 to +70°C
	MC68A52CP,CL	-40 to +85°C
2.0 MHz	MC68B52P,L	0 to +70°C

MC6852 SYNCHRONOUS SERIAL DATA ADAPTER
BLOCK DIAGRAM



A1.6 4802, 2716 MEMORY

PRELIMINARY

MOSTEK.

2K x 8 STATIC RAM

MK4802(P/J/N)*-1/3

FEATURES

- Static operation
- Organization: 2K x 8 bit RAM JEDEC pinout
- Pin compatible with Mostek's BYTEWYDE™ memory family
- Double density version of the MK4118 1K x 8 static RAM
- 24/28 pin ROM/PROM compatible pin configuration

Part No.	Access Time	R/W Cycle Time
MK4802-1	120 nsec	120 msec
MK4802-3	200 nsec	200 msec

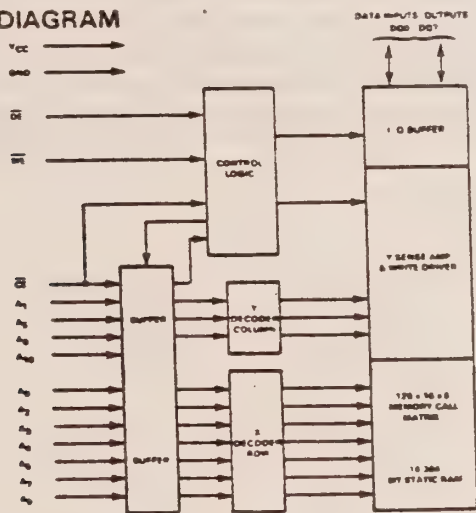
CE and OE functions facilitate bus control

DESCRIPTION

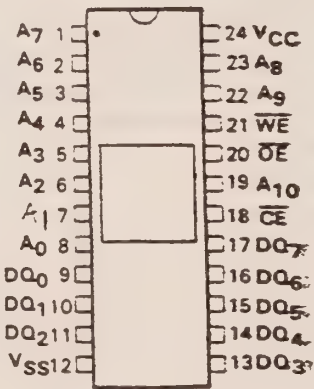
The MK4802 uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 16,384 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

Both the MK4802-1 and MK4802-3 present to the user a high density cost effective N-MOS memory with the performance characteristics necessary for today's high performance microprocessor applications. The MK4802 is ideal for memory applications where the organization requires relatively shallow depth with a wide word format.

BLOCK DIAGRAM



PIN CONNECTIONS



TRUTH TABLE

CE	OE	WE	Mode	DQ
VIH	X	X	Deselect	High Z
VIL	X	VIL	Write	DIN
VIL	VIL	VIH	Read	DOUT
VIL	VIH	VIH	Read	High Z

X = Don't Care

*See MK4802 Series data sheet for faster speeds

PIN NAMES

A0-A10	Address Inputs	VCC	Power (+5V)
CE	Chip Enable	WE	Write Enable
VSS	Ground	OE	Output Enable
DQ0-DQ7	Data In/Data Out		

MOSTEK®

2048 x 8-BIT EPROM

Electrically Programmable/Ultraviolet Erasable ROM

MK2716 (J)-5/6/7/8

FEATURES

- 16 384 Bit Ultraviolet Erasable, Electrically Programmable ROM, organized as 2048 words by 8 bits
- Single -5 volt power supply during READ operation
- Fast Access Time in READ mode

P/N	ACCESS TIME
MK2716-5	300ns
MK2716-6	350ns
MK2716-7	390ns
MK2716-8	450ns

- Low Power Dissipation: 525mW max active
- Power Down Mode: 132mW max standby
- Three State Output OR-tie capability

DESCRIPTION

The MK2716 is a 2048 x 8 bit electrically programmable/ultraviolet erasable Read Only Memory. The circuit is fabricated with Mostek's advanced N-channel silicon gate technology for the highest performance and reliability. The MK2716 offers significant advances over

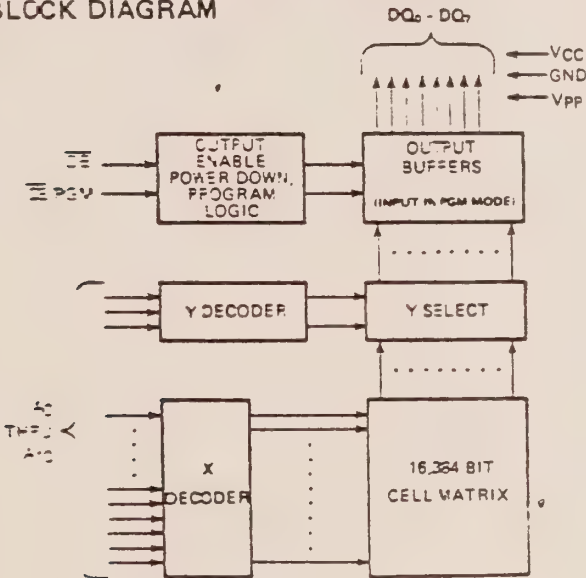
- Five modes of operation for greater system flexibility (see Table)
- Single programming requirement: single location programming with one 50msec pulse
- Pin Compatible with Mostek's BYTEWYDE™ Memory Family
- TTL compatible in all operating modes
- Standard 24 pin DIP with transparent lid

MODE SELECTION

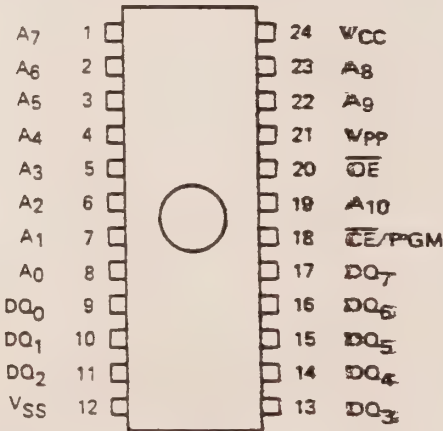
MODE	CE/PGM PIN	OE (20)	VPP (21)	OUTPUTS
READ	V _{IL}	V _{IL}	+5	Valid Out
STANDBY	V _{IH}	Don't Care	+5	Open
PROGRAM	Pulsed V _{IL} to V _{IH}	V _{IH}	+25	Input
PROGRAM VERIFY	V _{IL}	V _{IL}	+25	Valid Out
PROGRAM INHIBIT	V _{IL}	V _{IH}	+25	Open

V_{CC}(24) = 5V all modes

BLOCK DIAGRAM



PIN CONFIGURATION

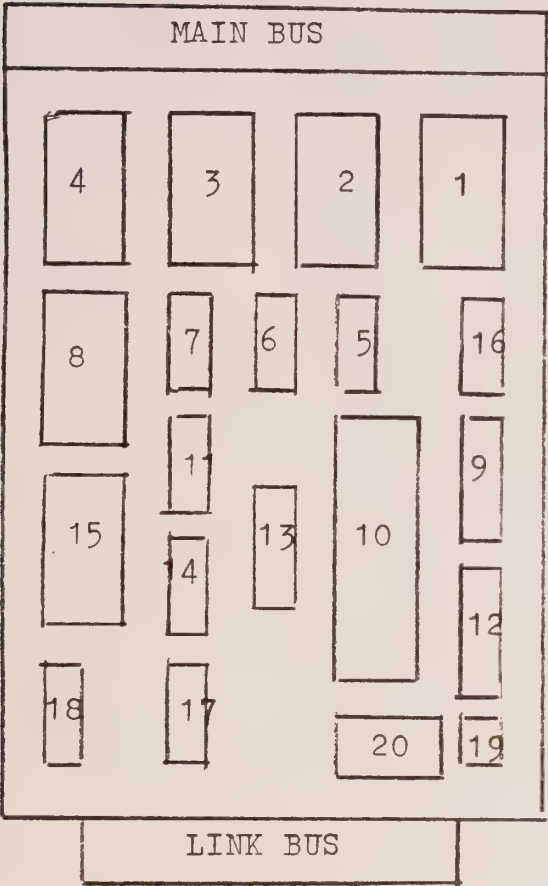


PIN NAMES

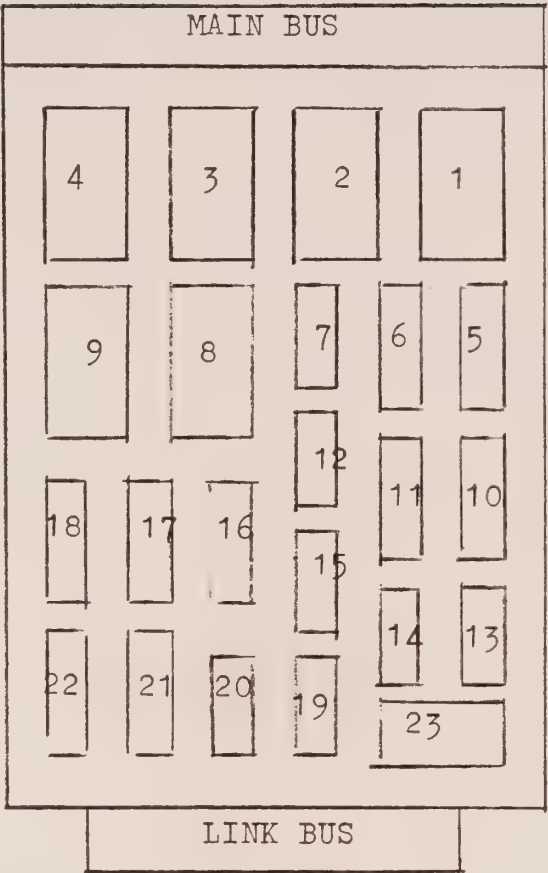
A0-A10	Addresses	DQ0-DQ7	Data Outputs*
CE/PGM	Chip Enable/ Program	OE	Output Enable
*Inputs in Program Mode		VSS	Ground

A2 COMPONENT PLACIG

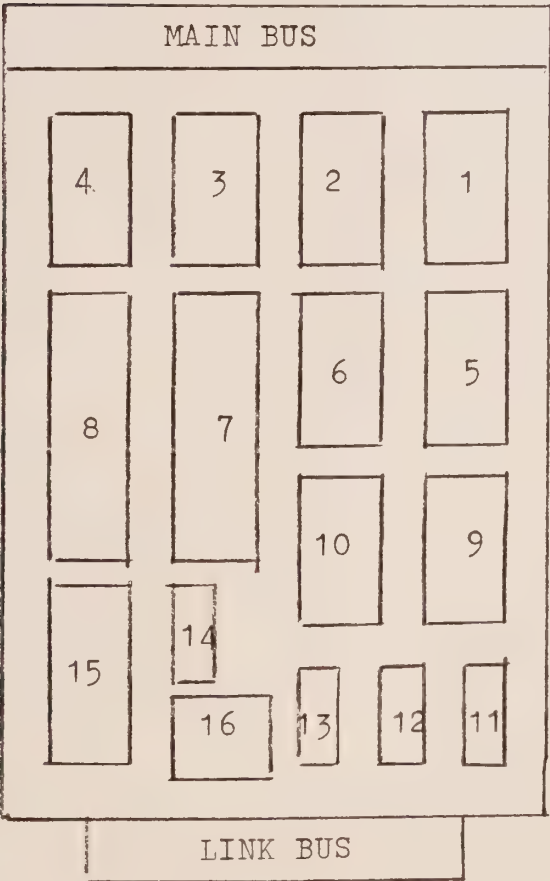
CPU BOARD



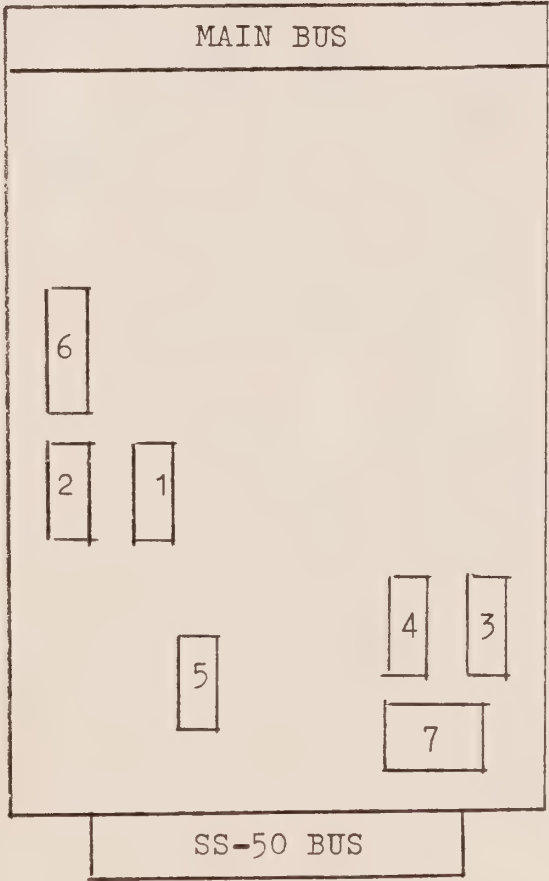
MEMORY BOARD



I/O BOARD



INTERFACE BOARD

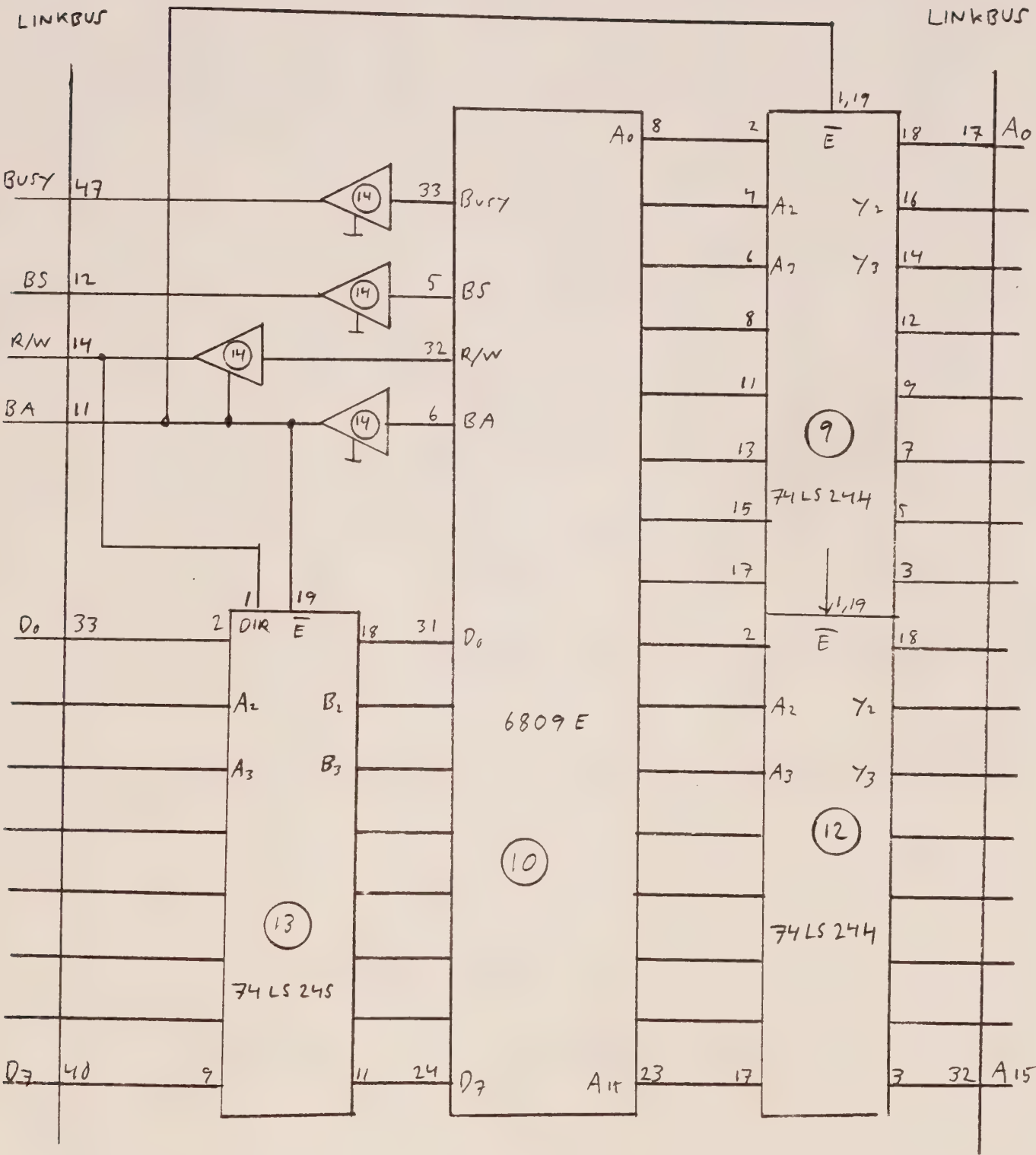


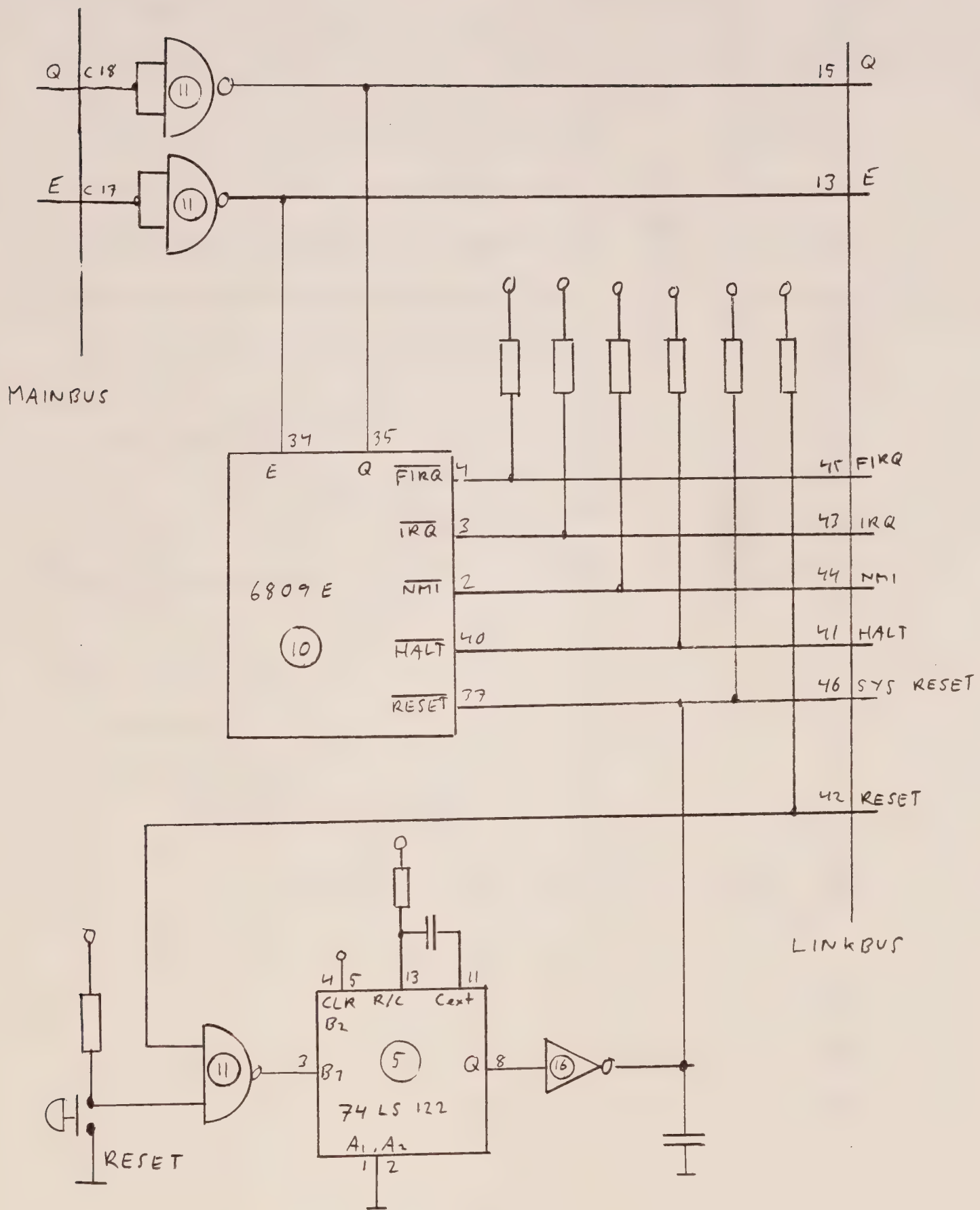
A3 PARTS LIST.

Name	Function	Quantity	Placing nr.
CPU board :			
2716	PROM	1 - 8	1 - 4, 8, 15
4802	RWM	1 - 8	1 - 4, 8, 15
6809E	CPU	1	10
74 LS 00	NAND	2	7, 11
74 LS 02	NOR	1	17
74 LS 05	INVERT O C	1	16
74 LS 125	3-State BUFFER	1	14
74 LS 138	3/8 DECODER	1	18
74 LS 221	MONOSTABLE M V	1	5
74 LS 244	BUS DRIVER	2	9, 12
74 LS 245	BUS DRIVER	1	13
7805	5 V SUPPLY	1	20
RESISTORS	PULL-UP, TIMING	8	6, 19
CAPACITORS	DECOUPLING, TIMING	8	6
I/O board :			
4802	MEMORY	1 - 8	1, 2, 5, 6, 9, 10
6821	PIA	2	7, 8
6840	TIMER	1	15
6850	ACIA	1	4
6852	SSDA	1	3
74 LS 00	NAND	1	12
74 LS 02	NOR	1	11
74 LS 138	3/8 DECODER	2	13, 14
7805	5 V SUPPLY	1	16
CAPACITORS	DECOUPLING	6	

Name	Function	Quantity	Placing nr.
Memory board :			
4802	MEMORY	1 - 8	1 - 4, 8, 9
74 LS 00	NAND	2	13, 19
74 LS 02	NOR	1	14
74 LS 05	INVERT O C	1	12
74 LS 74	FLIP-FLOP	1	15
74 LS 135	X-(N)OR	1	20
74 LS 138	3/8 DECODER	1	7
74 LS 241	BUS DRIVER	5	16 - 18, 21, 22
74 LS 244	BUS DRIVER	1	10
74 LS 245	BUS DRIVER	2	5, 6
74 LS 273	OCTAL FLIP-FLOP	1	11
7805	5 V SUPPLY	1	23
CAPACITORS	DECOUPLING	8	
Interface board :			
74 LS 14	INVERT	1	1
74 LS 138	3/8 DECODER	1	2
74 LS 241	BUS DRIVER	1	6
75188	RS-232 TRX	1	4
75189	RS-232 RX	1	3
7805	5 V SUPPLY	1	7
7812	12 V SUPPLY	1	5
7912	-12 V SUPPLY	1	5
RESISTOR	PULL-UP	1	5
CAPACITORS	DECOUPLING	6	5

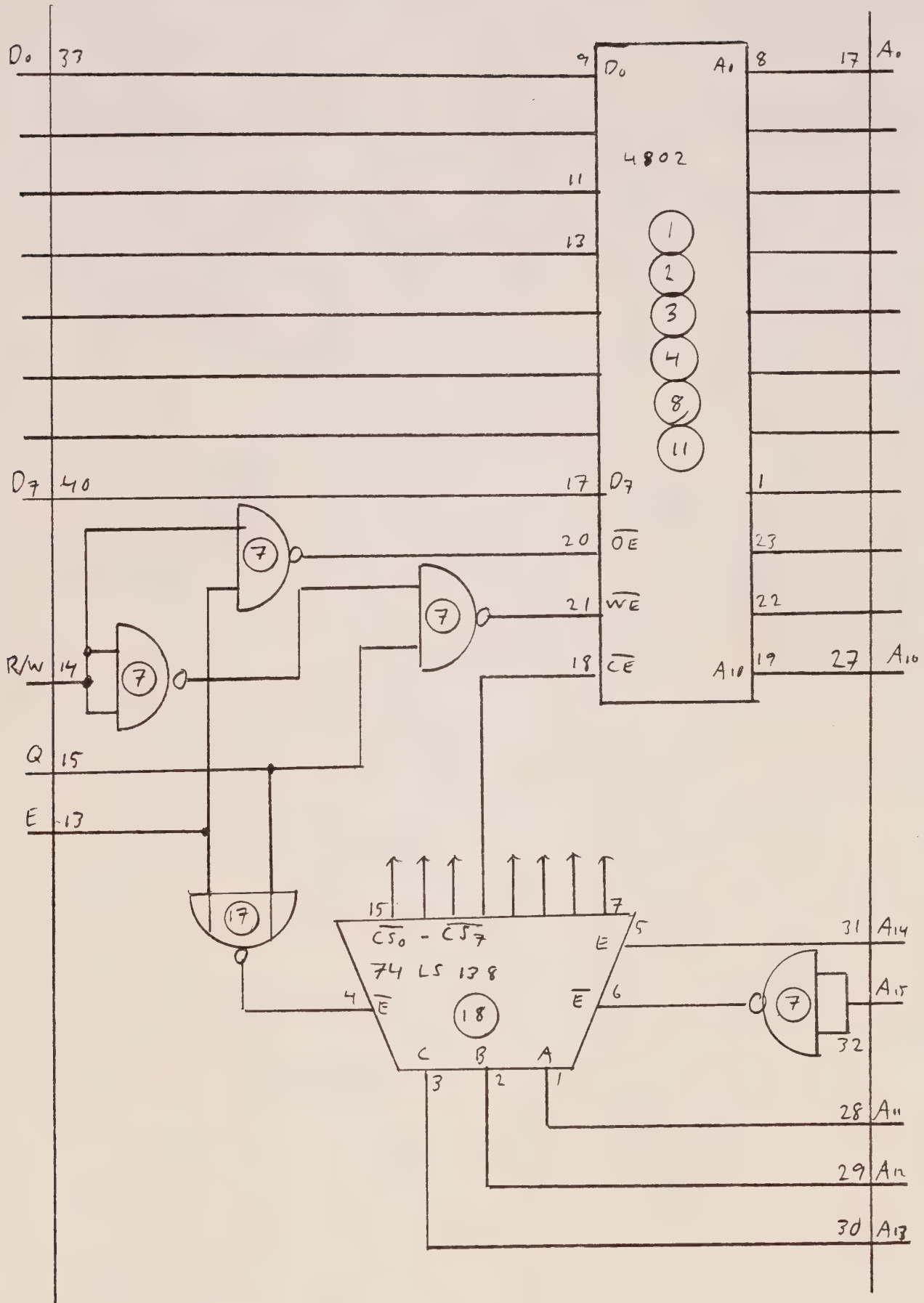
A4 SCHEMES
A4.1 CPU BOARD



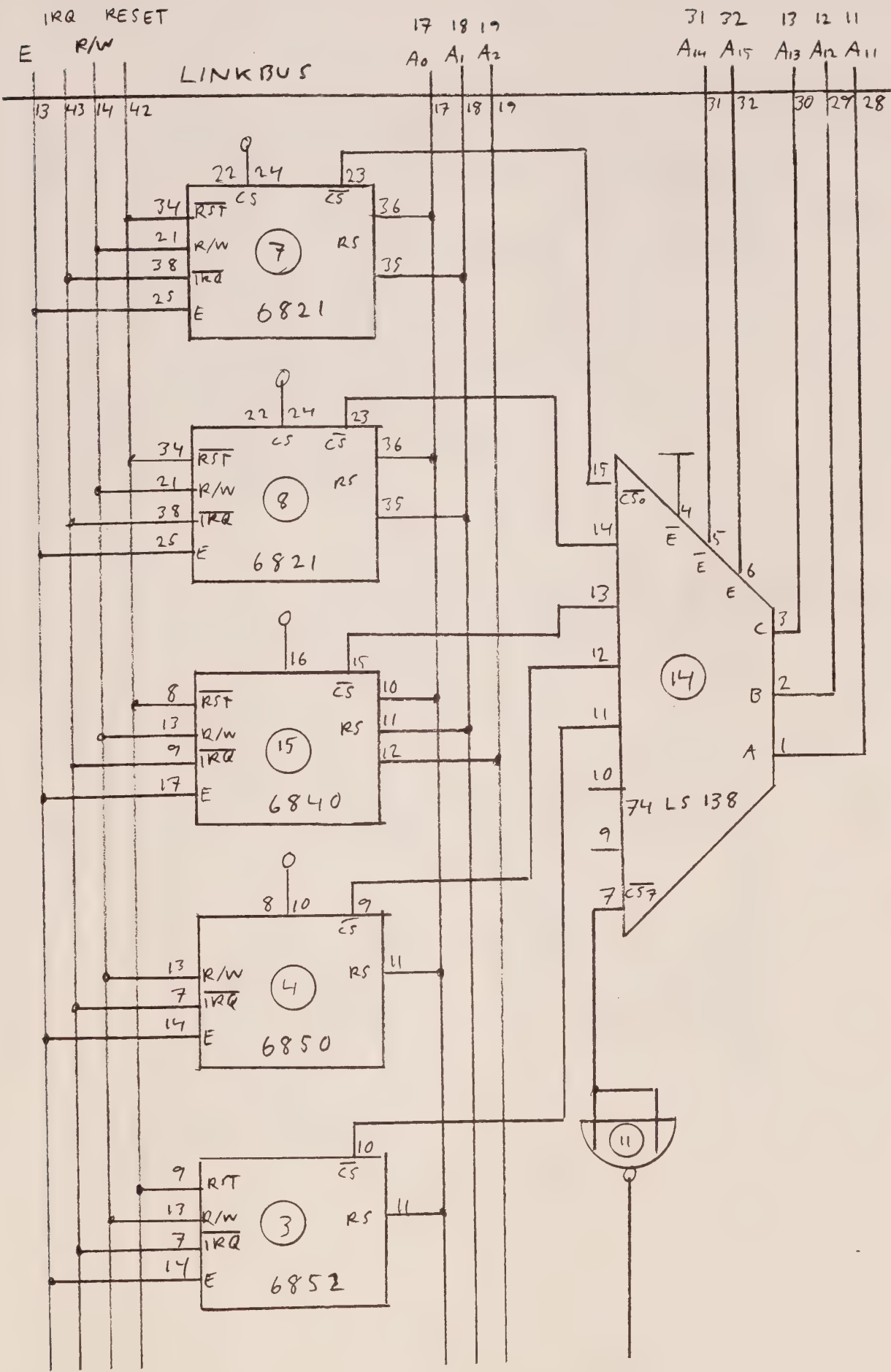


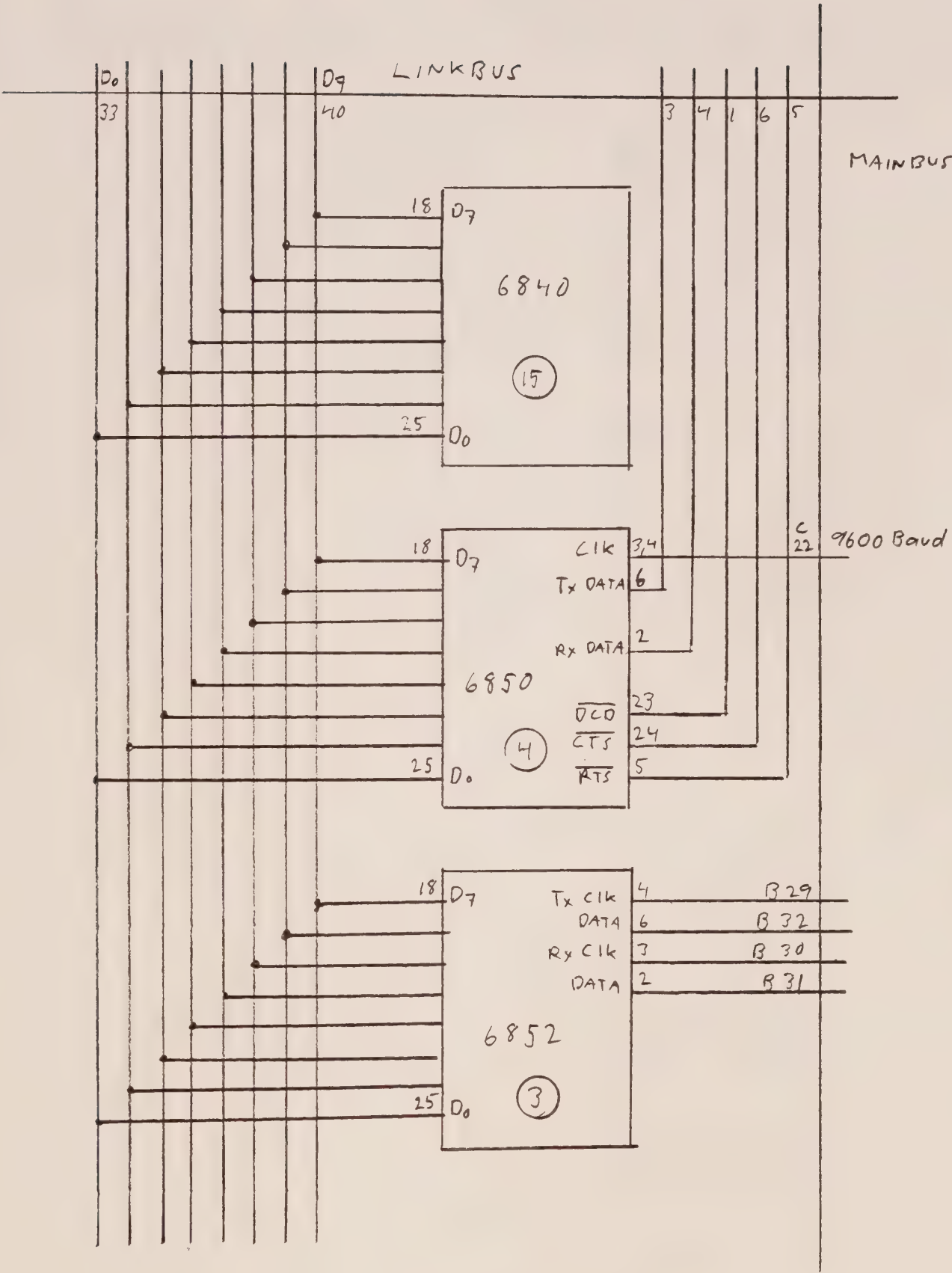
LINKBUS

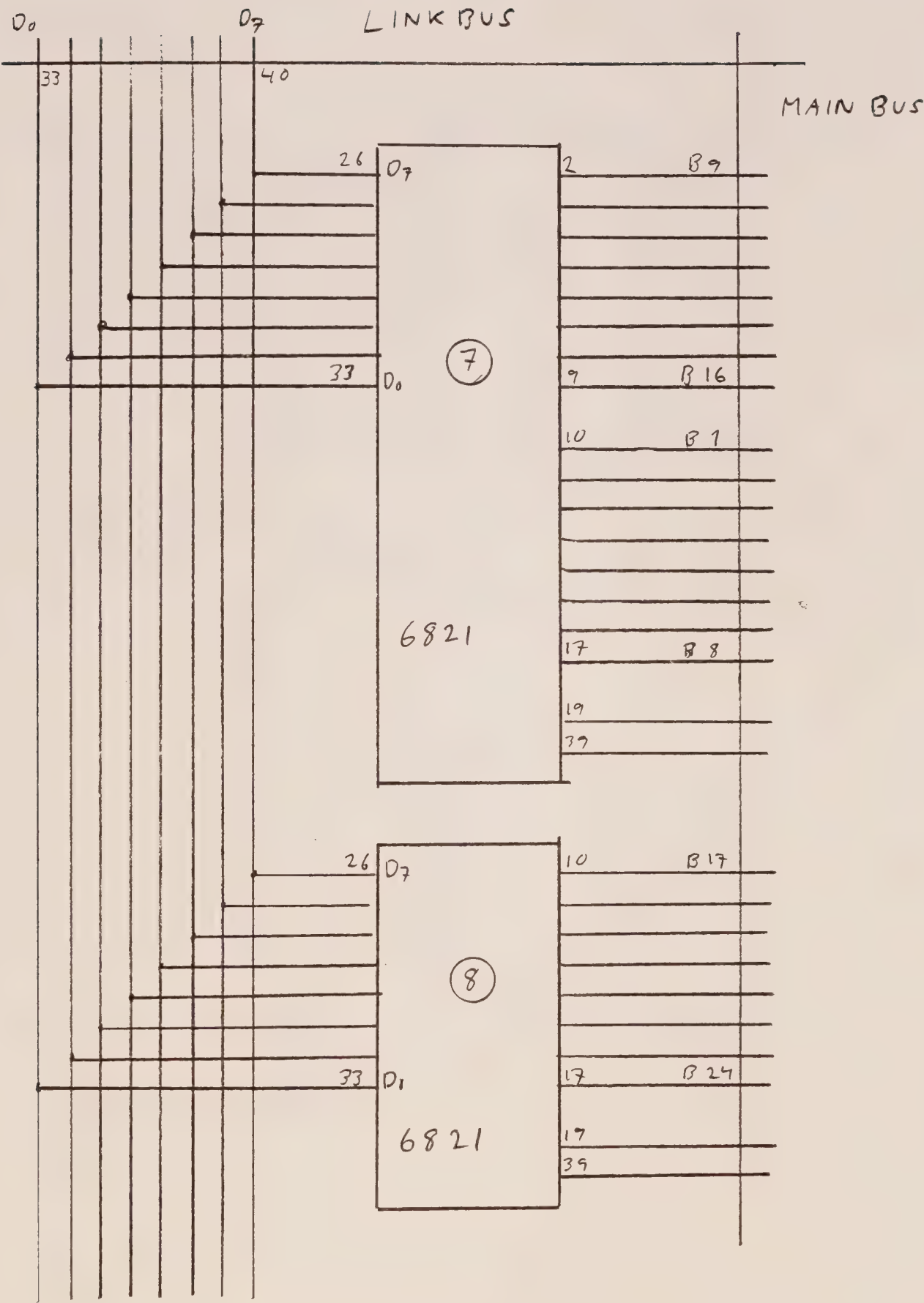
LINKBUS



A4.2 I/O BOARD

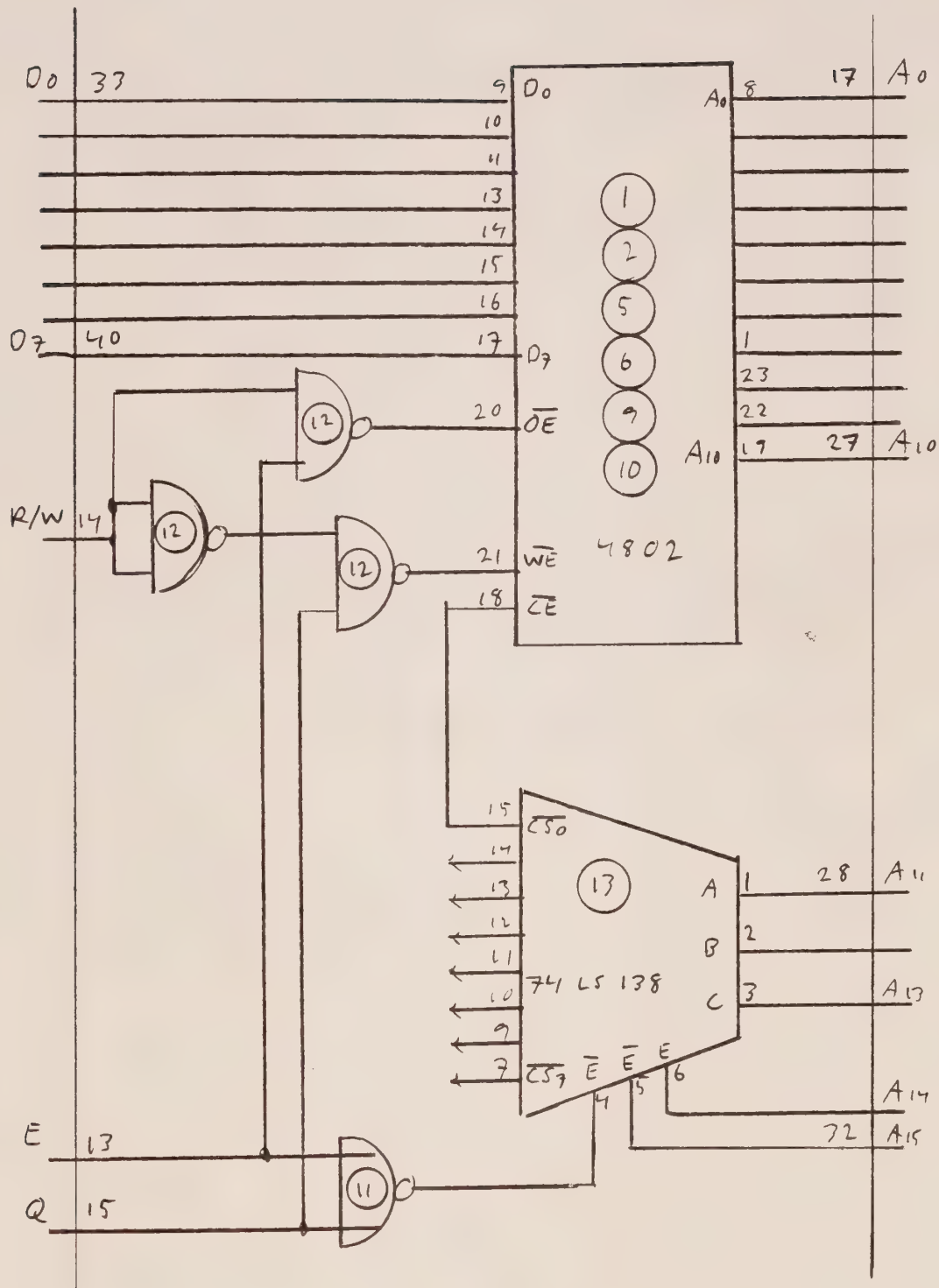




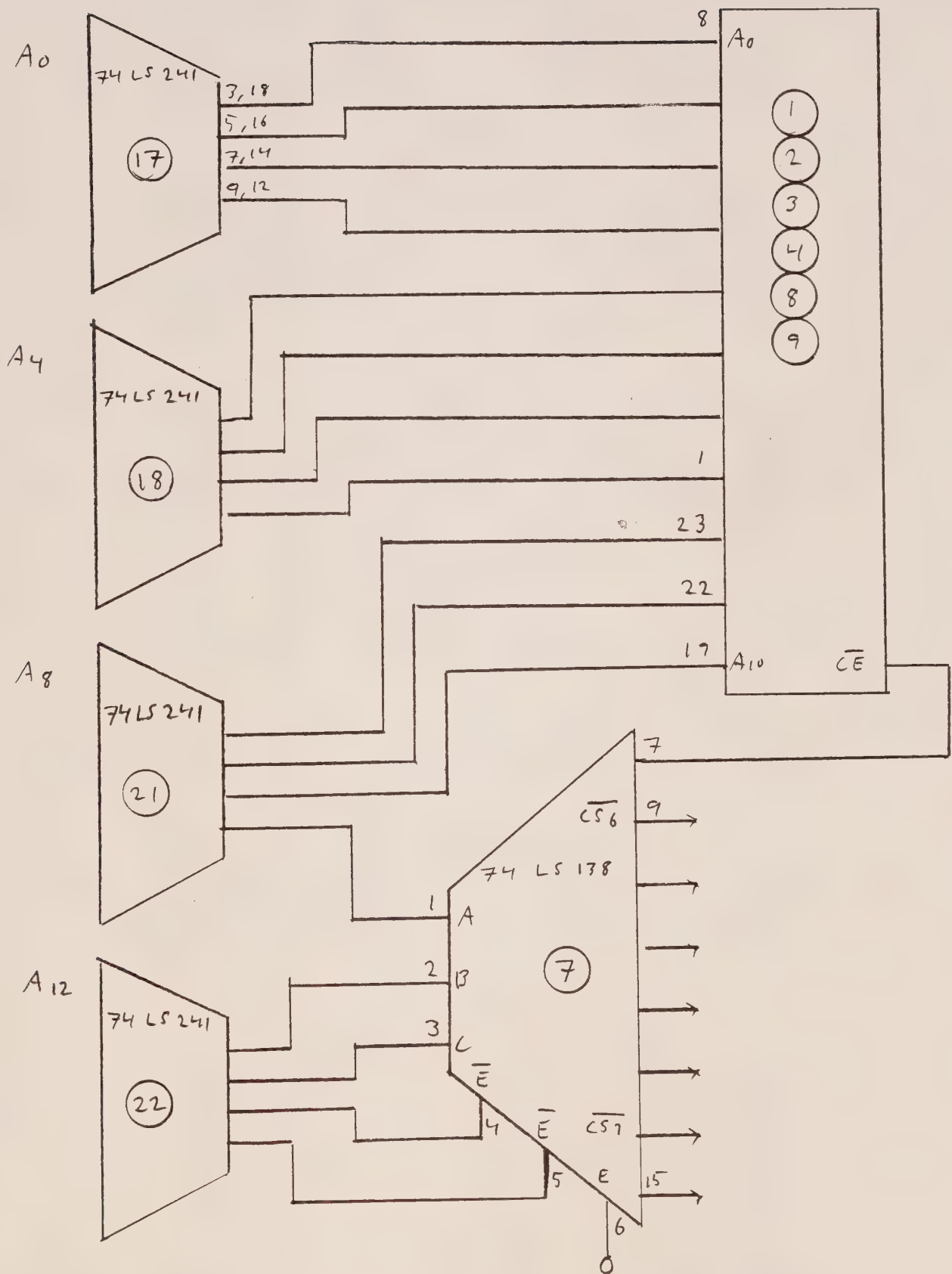


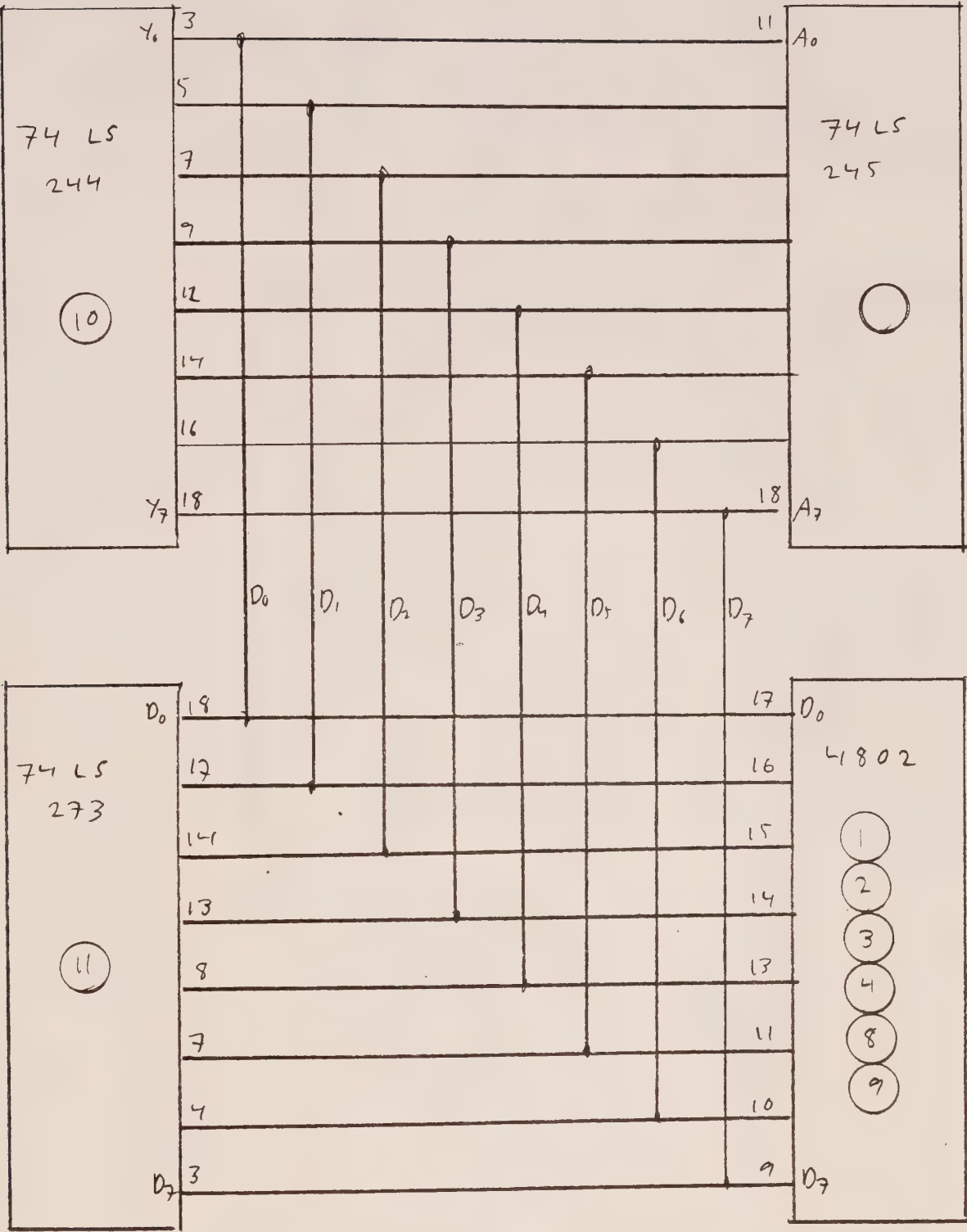
LINK BUS

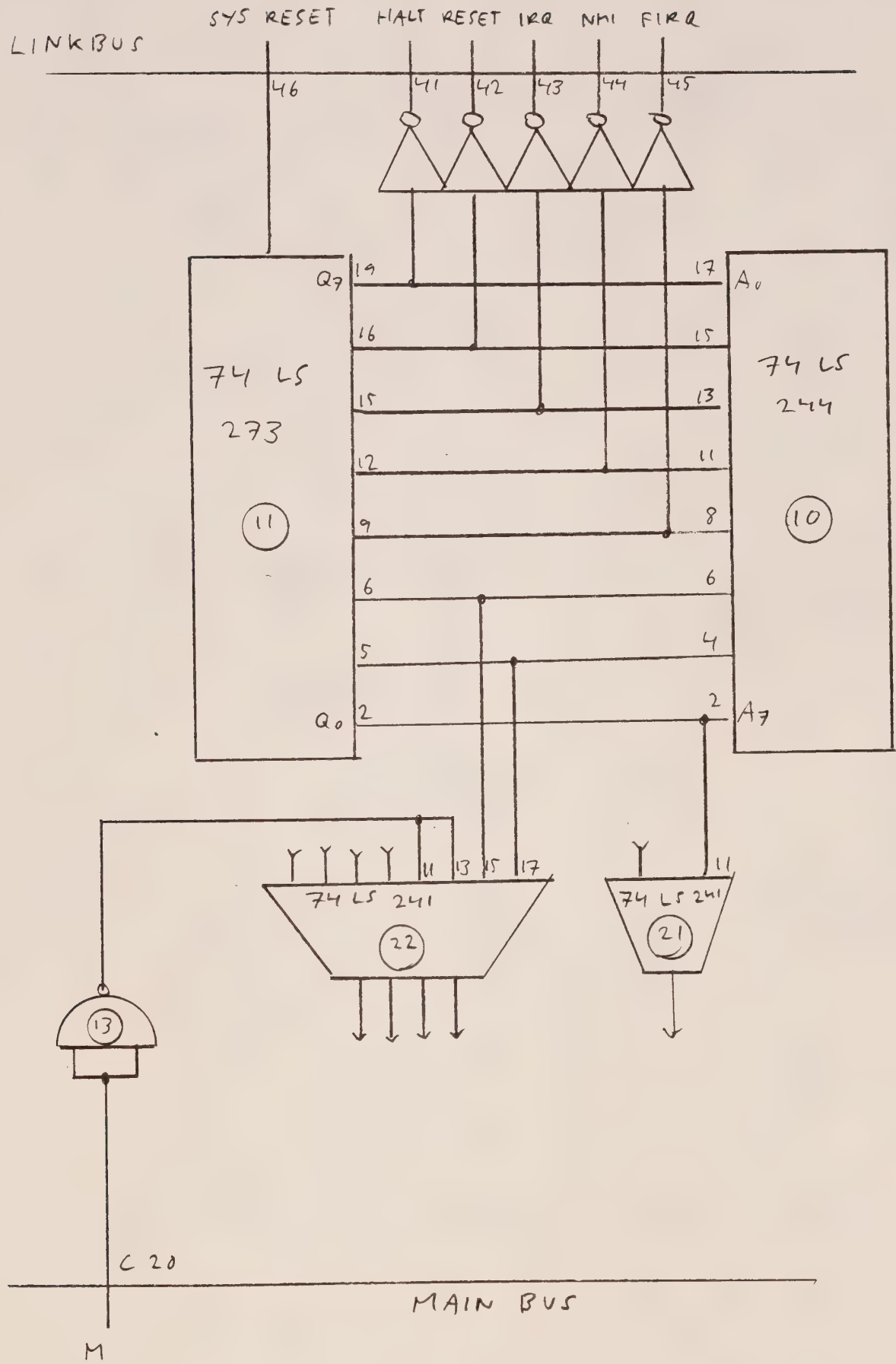
LINK BUS

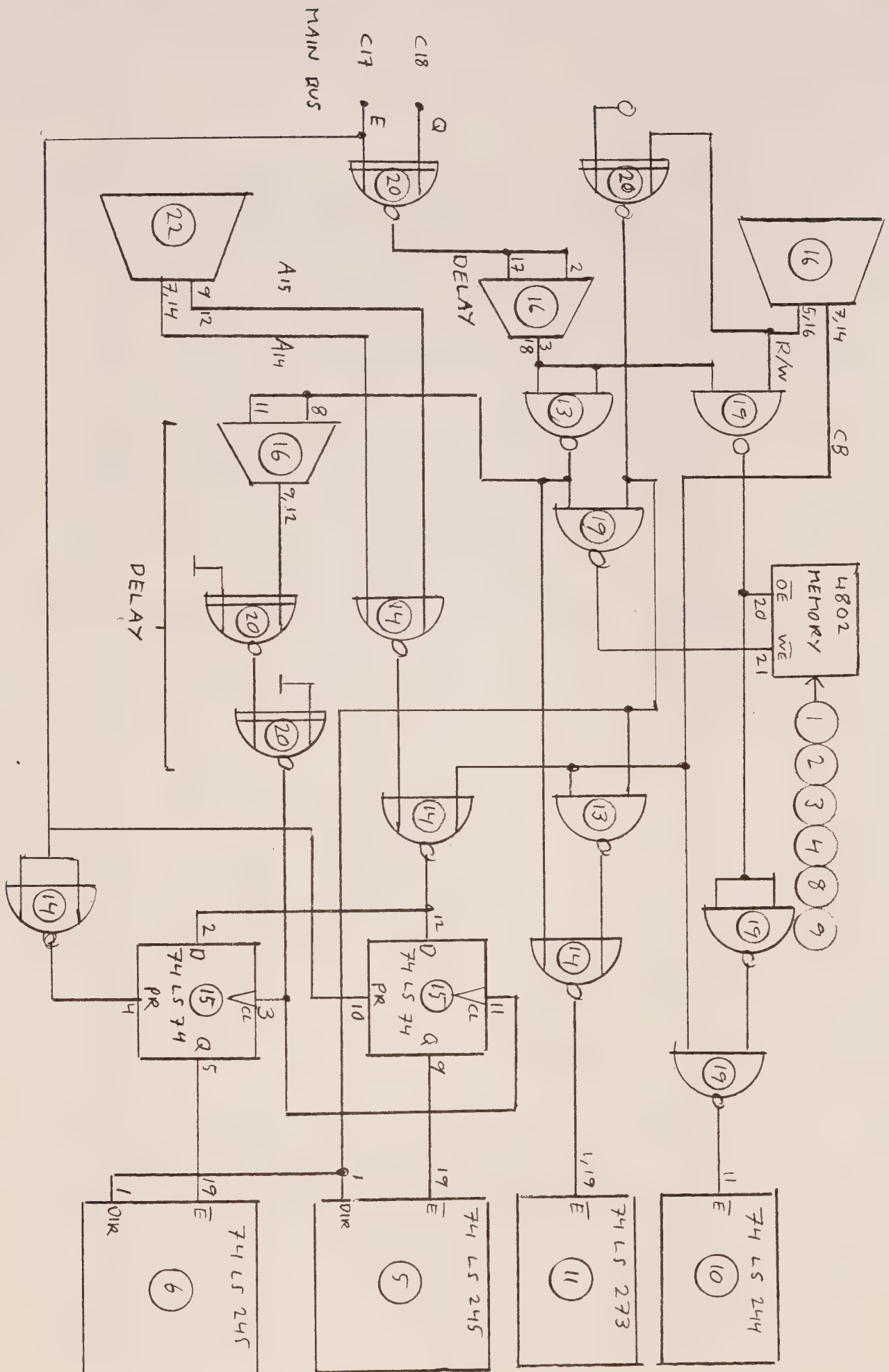


A4.3 MEMORY BOARD

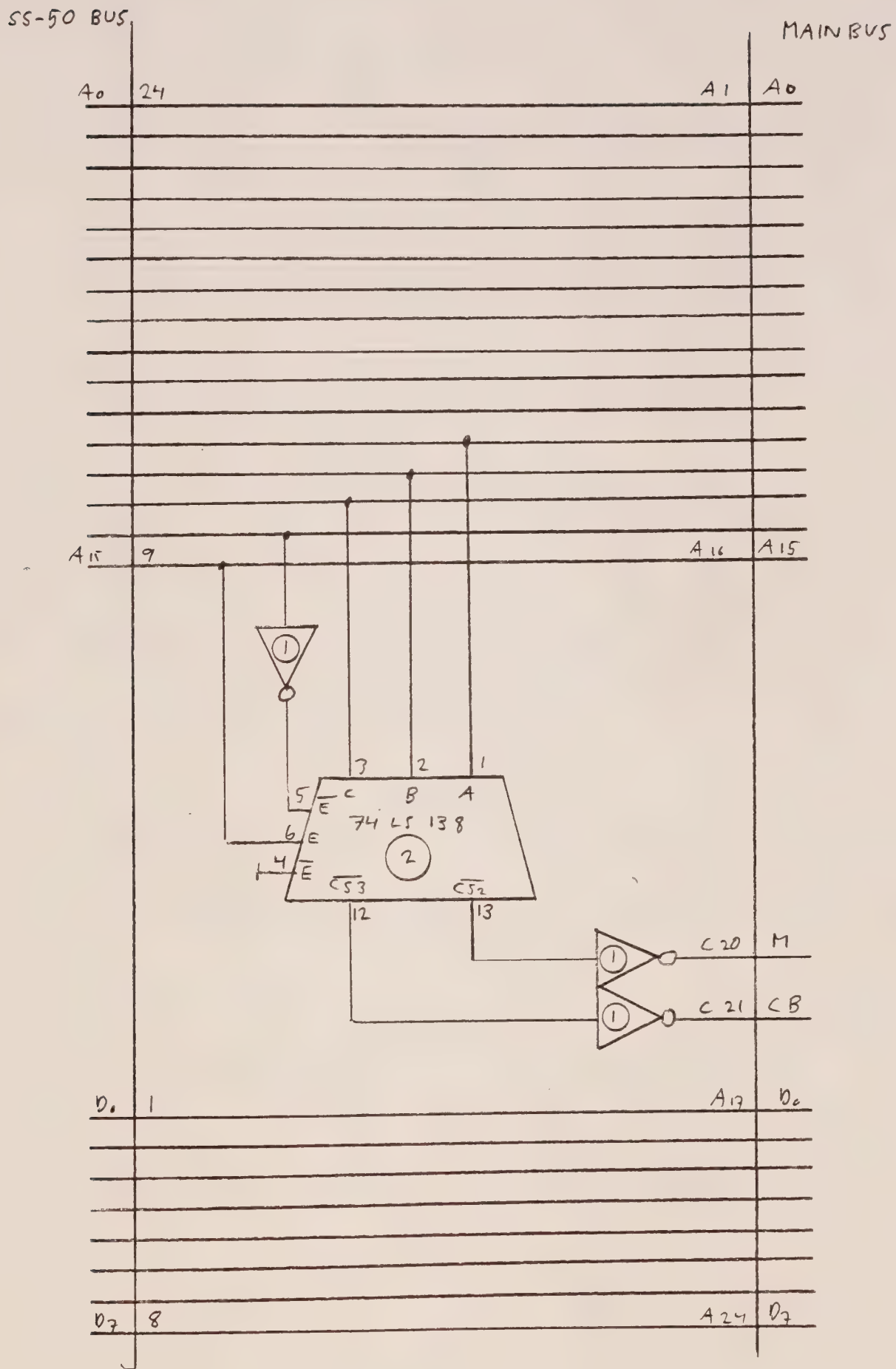


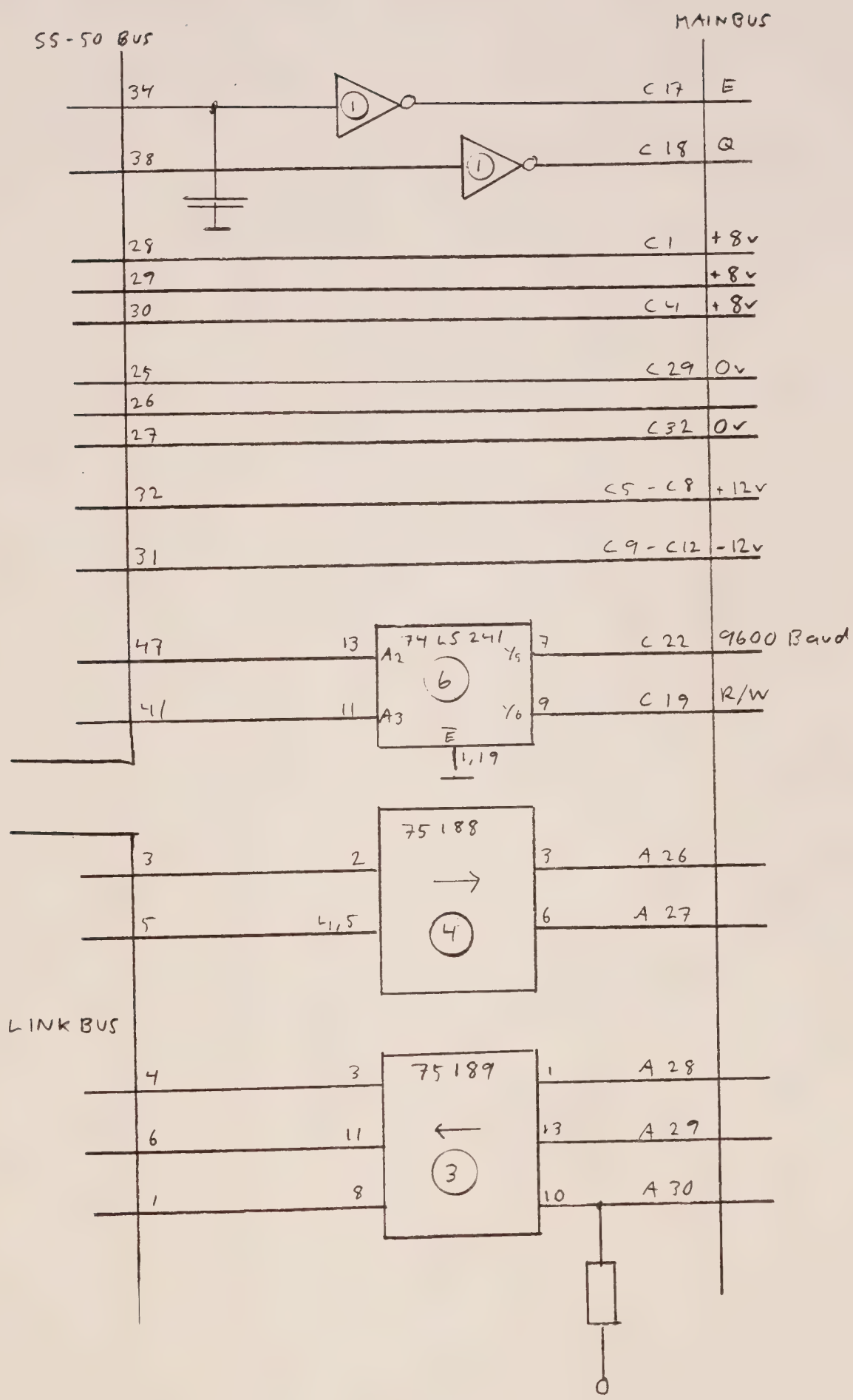






A4.4 INTERFACE BOARD





A5 BUSES

A5.1 MAIN BUS

NR	A BUS		B BUS		C BUS
	NODE COMPUTER		TRANSCIVER		CONTROL
1	ADDRESS	0	POWER	0	+8 V
2		1		1	"
3		2		2	"
4		3		3	"
5		4		4	+12 V
6		5		5	"
7		6		6	"
8		7		7	"
9		8	SIGNAL	0	-12 V
10		9		1	"
11		10		2	"
12		11		3	"
13		12		4	
14		13		5	
15		14		6	
16		15		7	
17	DATA	0	THRESHOLD	0	E CLOCK
18		1		1	Q CLOCK
19		2		2	R/W
20		3		3	M (memory)
21		4		4	CB (ctrl byte)
22		5		5	9600 BAUD
23		6		6	IRQ
24		7		7	HALT
25			CARRIER DETECT		
26	TTY TX DATA		TX / RX		
27	RTS				
28	RX DATA				
29	CTS		TX CLOCK		GND
30	DCD		RX CLOCK		"
31			RX DATA		"
32			TX DATA		"

A5.2 LINK BUS

NR	SIGNAL
1	ACIA DCD
2	
3	TX DATA
4	RX DATA
5	RTS
6	CTS
7	
8	
9	
10	
11	BA (bus available)
12	BS (bus status)
13	E CLOCK
14	R/W
15	Q CLOCK
16	CB (ctrl byte)
17	ADDRESS 0
18	1
19	2
20	3
21	4
22	5
23	6
24	7
25	8
26	9
27	10
28	11
29	12
30	13
31	14
32	15
33	DATA 0
34	1
35	2
36	3
37	4
38	5
39	6
40	7
41	HALT
42	RESET
43	IRQ
44	NMI
45	FIRQ
46	SYS RESET
47	BUSY
48	
49	
50	

A6 PROGRAM LISTINGS

8000	PIA1A	EQU	\$8000	PIAA #1
8002	PIA1B	EQU	\$8002	
8001	CRA1	EQU	\$8001	
8003	CRB1	EQU	\$8003	
8000	DDRA1	EQU	\$8000	
8002	DDRB1	EQU	\$8002	

8800	PIA2A	EQU	\$8800	PIAA #2
8802	PIA2B	EQU	\$8802	
8801	CRA2	EQU	\$8801	
8803	CRB2	EQU	\$8803	
8800	DDRA2	EQU	\$8800	
8802	DDRB2	EQU	\$8802	

9801	ACIA	EQU	\$9801	ACIA
9800	ACIACR	EQU	\$9800	
9800	ACISTA	EQU	\$9800	

A001	SSDA	EQU	\$A001	SSDA
A000	SSDCR1	EQU	\$A000	
A001	SSDCR2	EQU	\$A001	
A001	SSDCR3	EQU	\$A001	
A001	SSDSYN	EQU	\$A001	
A000	SSDSTA	EQU	\$A000	

F800			ORG	\$F800	
F800	4F		PIAINI	CLRA	INIT ROUTINE FOR PIA.
F801	B7	8001		STA	CRA1
F804	B7	8003		STA	CRB1
F807	B7	8801		STA	CRA2
F80A	B7	8803		STA	CRB2
F80D	B7	8000		STA	DDRA1
F810	43			COMA	
F811	B7	8002		STA	DDRB1
F814	B7	8802		STA	DDRB2
F817	86	02		LDA	#\$2
F819	B7	8800		STA	DDRA2
F81C	86	04		LDA	#\$4
F81E	B7	8001		STA	CRA1
F821	B7	8003		STA	CRB1
F824	B7	8801		STA	CRA2
F827	B7	8803		STA	CRB2
F82A	39			RTS	
F82B	86	03	ACIINI	LDA	#\$3
F82D	B7	9800		STA	ACIACR
F830	86	15		LDA	#\$15
F832	B7	9800		STA	ACIACR
F835	39			RTS	
F836	86	03	SSDINI	LDA	#\$3
F838	B7	A000		STA	SSDCR1
F83B	86	5C		LDA	#\$5C
F83D	B7	A001		STA	SSDCR2
F840	86	40		LDA	#\$40
F842	B7	A000		STA	SSDCR1
F845	86	03		LDA	#\$3
F847	B7	A001		STA	SSDCR3
F84A	86	80		LDA	#\$80
F84C	B7	A000		STA	SSDCR1
F84F	86	16		LDA	#\$16
F851	B7	A001		STA	SSDSYN
F854	86	C4		LDA	#\$C4
F856	B7	A000		STA	SSDCR1
F859	39			RTS	

F900			ORG	\$F900	
F900	10CE	4800	RESET	LDS	#\$4800
F904	CE	4700		LDU	#\$4700
F907	BD	F800		JSR	PIAINI
F90A	BD	F82B		JSR	ACIINI
F90D	BD	F836		JSR	SSDINI
F910	7E	FA00		JMP	MONTOR
F920			ORG	\$F920	
F920	3B		NMI	RTI	INTERRUPT ROUTINES.
F940			ORG	\$F940	
F940	3B		SWI	RTI	
F960			ORG	\$F960	
F960	3B		IRQ	RTI	
F980			ORG	\$F980	
F980	3B		FIRQ	RTI	
F9A0			ORG	\$F9A0	
F9A0	3B		SWI2	RTI	
FOC0			ORG	\$FOC0	
FOC0	3B		SWI3	RTI	

FA00			ORG	\$FA00	
FA00 BD	FADD	MONTOR	JSR	PCRLF	MONITOR.
FA03 86	40		LDA	#\$40	
FA05 BD	FAFF		JSR	OUTCH	
FA08 86	20		LDA	#\$20	
FA0A BD	FAFF		JSR	OUTCH	
FA0D BD	FAF7		JSR	INCHE	
FA10 81	4D		CMPA	#\$4D	(M)
FA12 27	15		BEQ	MEMDIS	
FA14 81	50		CMPA	#\$50	(P)
FA16 27	07		BEQ	PROGC	
FA18 81	47		CMPA	#\$47	(G)
FA1A 27	0B		BEQ	GO	
>FA1C 7E	FA00		JMP	MONTOR	
FA1F 86	3A	PROGC	LDA	#\$3A	WRITE `:`
FA21 BD	FAFF		JSR	OUTCH	
>FA24 BD	FA98		JSR	RDADR	
FA27 6E	84	GO	JMP	,X	JUMP.
FA29 86	20	MEMDIS	LDA	#\$20	DISPLAY MEMORY.
FA2B BD	FAFF		JSR	OUTCH	
>FA2E BD	FA98		JSR	RDADR	
FA31 BD	FADD	M1	JSR	PCRLF	
FA34 BD	FACC		JSR	WRADR	
FA37 86	20		LDA	#\$20	
FA39 BD	FAFF		JSR	OUTCH	
FA3C A6	80		LDA	,X+	
>FA3E BD	FAAB		JSR	WRTNUM	
FA41 86	20		LDA	#\$20	
FA43 BD	FAFF		JSR	OUTCH	
FA46 BD	FAEC		JSR	INCH	
FA49 81	16		CMPA	#\$16	↓
FA4B 27	E4		BEQ	M1	
FA4D 81	0B		CMPA	#\$0B	↑
FA4F 26	05		BNE	M4	
FA51 A6	83		LDA	,--X	
>FA53 7E	FA31		JMP	M1	
FA56 81	30	M4	CMPA	#\$30	(O)
FA58 2D	A6		BLT	MONTOR	
FA5A 81	46		CMPA	#\$46	(F)
FA5C 2E	A2		BGT	MONTOR	
FA5E BD	FAFF		JSR	OUTCH	
>FA61 BD	FA71		JSR	A2	
>FA64 BD	FA82		JSR	R1	
FA67 A7	82		STA	, -X	
FA69 A6	80		LDA	,X+	
>FA6B 7E	FA31		JMP	M1	
FA6E BD	FAF7	ASC	JSR	INCHE	READ HEX DIGIT.
FA71 80	40	A2	SUBA	#\$40	
FA73 2C	02		BGE	A1	
FA75 8B	07		ADDA	#\$7	
FA77 8B	09	A1	ADDA	#\$9	
FA79 39			RTS		

FA7A	34	04	RDNUM	PSHS	B	READ HEX NR.
>FA7C	BD	FA6E		JSR	ASC	
>FA7F	7E	FA84		JMP	R2	
FA82	34	04	R1	PSHS	B	
FA84	1F	89	R2	TFR	A,B	
>FA86	BD	FA6E		JSR	ASC	
FA89	48			LSLA		
FA8A	48			LSLA		
FA8B	48			LSLA		
FA8C	48			LSLA		
FA8D	56			RORB		
FA8E	46			RORA		
FA8F	56			RORB		
FA90	46			RORA		
FA91	56			RORB		
FA92	46			RORA		
FA93	56			RORB		
FA94	46			RORA		
FA95	35	04		PULS	B	
FA97	39			RTS		
FA98	34	06	RDADR	PSHS	D	READ HEX ADDRESS.
>FA9A	BD	FA7A		JSR	RDNUM	
FA9D	34	02		PSHS	A	
>FA9F	BD	FA7A		JSR	RDNUM	
FAA2	1F	89		TFR	A,B	
FAA4	35	02		PULS	A	
FAA6	1F	01		TFR	D,X	
FAA8	35	06		PULS	D	
FAAA	39			RTS		
FAAB	34	04	WRTNUM	PSHS	B	WRITE HEX NR.
FAAD	1F	89		TFR	A,B	
FAAF	C4	0F		ANDB	#\$0F	
FAB1	44			LSRA		
FAB2	44			LSRA		
FAB3	44			LSRA		
FAB4	44			LSRA		
>FAB5	BD	FACO		JSR	WRSR	
FAB8	1F	98		TFR	B,A	
>FABA	BD	FACO		JSR	WRSR	
FABD	35	04		PULS	B	
FABF	39			RTS		
FAC0	81	09	WRSR	CMPA	#\$9	WRITE HEX DIGIT.
FAC2	2E	02		BGT	W1	
FAC4	80	07		SUBA	#\$7	
FAC6	8B	37	W1	ADLA	#\$37	
>FAC8	BD	FAFF		JSR	OUTCH	
FACB	39			RTS		

FACC 34	06	WRADR	PSHS	D	WRITE HEX ADRESS
FACE 1F	10		TFR	X,D	
>FAD0 BD	FAAB		JSR	WRTNUM	
FAD3 1F	10		TFR	X,D	
FAD5 1F	98		TFR	B,A	
>FAD7 BD	FAAB		JSR	WRTNUM	
FADA 35	06		PULS	D	
FADC 39			RTS		
FADD 34	02	PCRLF	PSHS	A	CR, LF.
FADF 86	0D		LDA	#\$0D	
>FAE1 BD	FAFF		JSR	OUTCH	
FAE4 86	0A		LDA	#\$0A	
>FAE6 BD	FAFF		JSR	OUTCH	
FAE9 35	02		PULS	A	
FAEB 39			RTS		
FAEC B6	9800	INCH	LDA	ACISTA	READ CHARACTER.
FAEF 85	01		BITA	#\$01	
FAF1 27	F9		BEQ	INCH	
FAF3 B6	9801		LDA	ACIA	
FAF6 39			RTS		
>FAF7 BD	FAEC	INCHE	JSR	INCH	READ AND ECHO.
FAFA 84	7F		ANDA	#\$7F	
>FAFC 7E	FAFF		JMP	OUTCH	
FAFF 34	04	OUTCH	PSHS	B	WRITE CHARACTER.
FB01 F6	9800	01	LDB	ACISTA	
FB04 C5	02		BITB	#\$02	
FB06 27	F9		BEQ	01	
FB08 B7	9801		STA	ACIA	
FB0B 35	04		PULS	B	
FB0D 39			RTS		
FFF2			ORG	FFFF2	
FFF2 F0C0			FDB	SWI3	INTERRUPT VECTOR.
FFF4 F9A0			FDB	SWI2	
FFF6 F980			FDB	FIRQ	
FFF8 F960			FDB	IRQ	
FFFA F940			FDB	SWI	
FFFC F920			FDB	NMI	
FFFE F900			FDB	RESET	
			END		

A7 LINK MEMORY MAP

